

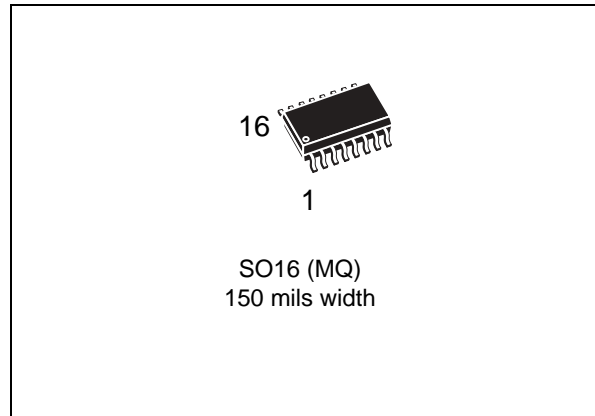


## CR14

### Low Cost ISO14443 type-B Contactless Coupler Chip with Anti-Collision and CRC Management

#### Features summary

- Single 5V  $\pm$ 500mV Supply Voltage
- SO16N package
- Contactless Communication
  - ISO14443 type-B protocol
  - 13.56MHz Carrier Frequency using an External Oscillator
  - 106 Kbit/s Data Rate
  - 36 Byte Input/Output Frame Register
  - Supports Frame Answer with/without SOF/EOF
  - CRC Generation and Check
  - Automated ST Anti-Collision Exchange
- I<sup>2</sup>C Communication
  - Two Wire I<sup>2</sup>C Serial Interface
  - Supports 400kHz Protocol
  - 3 Chip Enable Pins
  - Up to 8 CR14 Connected on the Same Bus



# Contents

<b>1</b>	<b>Summary description</b> .....	<b>6</b>
<b>2</b>	<b>Signal description</b> .....	<b>9</b>
2.1	Oscillator (OSC1, OSC2) .....	9
2.2	Antenna Output Driver (RF <sub>OUT</sub> ) .....	9
2.3	Antenna Input Filter (RF <sub>IN</sub> ) .....	9
2.4	Transmitter Reference Voltage (V <sub>REF</sub> ) .....	9
2.5	Serial Clock (SCL) .....	9
2.6	Serial Data (SDA) .....	10
2.7	Chip Enable (E0, E1, E2) .....	10
2.8	Power Supply (V <sub>CC</sub> , GND, GND <sub>RF</sub> ) .....	10
<b>3</b>	<b>CR14 registers</b> .....	<b>12</b>
3.1	Parameter Register (00h) .....	13
3.2	Input/Output Frame Register (01h) .....	13
3.3	Slot Marker Register (03h) .....	14
<b>4</b>	<b>CR14 I<sup>2</sup>C protocol description</b> .....	<b>16</b>
4.1	I <sup>2</sup> C Start Condition .....	17
4.2	I <sup>2</sup> C Stop Condition .....	17
4.3	I <sup>2</sup> C Acknowledge Bit (ACK) .....	17
4.4	I <sup>2</sup> C Data Input .....	17
4.5	I <sup>2</sup> C Memory Addressing .....	18
4.6	CR14 I <sup>2</sup> C Write Operations .....	19
4.7	CR14 I <sup>2</sup> C Read Operations .....	21
<b>5</b>	<b>Applying the I<sup>2</sup>C protocol to the CR14 registers</b> .....	<b>22</b>
5.1	I <sup>2</sup> C Parameter Register Protocol .....	22
5.2	I <sup>2</sup> C Input/Output Frame Register Protocol .....	23
5.3	I <sup>2</sup> C Slot Marker Register Protocol .....	24
5.4	Addresses above Location 06h .....	25

- 6 CR14 ISO14443 type-B Radio Frequency data transfer . . . . . 26**
  - 6.1 Output RF Data Transfer from the CR14 to the PICC (Request Frame) . . . . . 26
  - 6.2 Transmission Format of Request Frame Characters . . . . . 27
  - 6.3 Request Start Of Frame . . . . . 27
  - 6.4 Request End Of Frame . . . . . 28
  - 6.5 Input RF Data Transfer from the PICC to the CR14 (Answer Frame) . . . . . 28
  - 6.6 Transmission Format of Answer Frame Characters . . . . . 29
  - 6.7 Answer Start Of Frame . . . . . 29
  - 6.8 Answer End Of Frame . . . . . 29
  - 6.9 Transmission Frame . . . . . 30
  - 6.10 CRC . . . . . 30
  
- 7 Tag access using the CR14 coupler . . . . . 31**
  - 7.1 Standard TAG Command Access Description . . . . . 31
  - 7.2 Anti-Collision TAG Sequence . . . . . 32
  
- 8 Maximum rating . . . . . 35**
  
- 9 DC and AC parameters . . . . . 36**
  
- 10 Package mechanical . . . . . 42**
  
- 11 Part numbering . . . . . 43**
  
- Appendix A ISO14443 type B CRC calculation . . . . . 44**
  
- 12 Revision history . . . . . 45**

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## List of tables

Table 1.	Signal Names . . . . .	7
Table 2.	CR14 Control Registers . . . . .	12
Table 3.	Parameter Register Bits Description . . . . .	13
Table 4.	Input/Output Frame Register Description . . . . .	14
Table 5.	Slot Marker Register Description . . . . .	15
Table 6.	Device Select Code . . . . .	16
Table 7.	CR14 Request Frame Character Format . . . . .	27
Table 8.	Absolute Maximum Ratings . . . . .	35
Table 9.	I <sup>2</sup> C AC Measurement Conditions . . . . .	36
Table 10.	I <sup>2</sup> C Input Parameters(1,2) . . . . .	36
Table 11.	I <sup>2</sup> C DC Characteristics . . . . .	37
Table 12.	I <sup>2</sup> C AC Characteristics . . . . .	39
Table 13.	RF <sub>OUT</sub> AC Characteristics . . . . .	41
Table 14.	RF <sub>IN</sub> AC Characteristics . . . . .	41
Table 15.	SO16 Narrow - 16 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data . . . . .	42
Table 16.	Ordering Information Scheme. . . . .	43
Table 17.	Document Revision History . . . . .	45

## List of figures

Figure 1.	Logic Diagram	7
Figure 2.	Logic Block Diagram	8
Figure 3.	SO Pin Connections	8
Figure 4.	CR14 Application Schematic	10
Figure 5.	Maximum $R_L$ Value versus Bus Capacitance ( $C_{BUS}$ ) for an I <sup>2</sup> C Bus	11
Figure 6.	I <sup>2</sup> C Bus Protocol	18
Figure 7.	CR14 I <sup>2</sup> C Write Mode Sequence	19
Figure 8.	I <sup>2</sup> C Polling Flowchart using ACK	20
Figure 9.	CR14 I <sup>2</sup> C Read Modes Sequences	21
Figure 10.	Host-to-CR14 Transfer: I <sup>2</sup> C Write to Parameter Register	22
Figure 11.	CR14-to-Host Transfer: I <sup>2</sup> C Random Address Read from Parameter Register	22
Figure 12.	CR14-to-Host Transfer: I <sup>2</sup> C Current Address Read from Parameter Register	22
Figure 13.	Host-to-CR14 Transfer: I <sup>2</sup> C Write to Input/Output Frame Register for ISO14443B	23
Figure 14.	CR14-to-Host Transfer: I <sup>2</sup> C Random Address Read from Input/Output Frame Register for ISO14443B	23
Figure 15.	CR14-to-Host Transfer: I <sup>2</sup> C Current Address Read from I/O Frame Register for ISO14443B	24
Figure 16.	Host-to-CR14 Transfer: I <sup>2</sup> C Write to Slot Marker Register	24
Figure 17.	CR14-to-Host Transfer: I <sup>2</sup> C Random Address Read from Slot Marker Register	25
Figure 18.	CR14-to-Host Transfer: I <sup>2</sup> C Current Address Read from Slot Marker Register	25
Figure 19.	Wave Transmitted using ASK Modulation	26
Figure 20.	CR14 Request Frame Character Format	27
Figure 21.	Request Start Of Frame	27
Figure 22.	Request End Of Frame	28
Figure 23.	Wave Received using BPSK Sub-carrier Modulation	28
Figure 24.	Answer Start Of Frame	29
Figure 25.	Answer End Of Frame	29
Figure 26.	Example of a Complete Transmission Frame	30
Figure 27.	CRC Transmission Rules	30
Figure 28.	Standard TAG Command: Request Frame Transmission	31
Figure 29.	Standard TAG Command: Answer Frame Reception	32
Figure 30.	Standard TAG Command: Complete TAG Access Description	32
Figure 31.	Anti-Collision ST short range memory Sequence (1)	33
Figure 32.	Anti-Collision ST short range memory Sequence Continued	34
Figure 33.	I <sup>2</sup> C AC Testing I/O Waveform	36
Figure 34.	I <sup>2</sup> C AC Waveforms	38
Figure 35.	CR14 Synchronous Timing	40
Figure 36.	SO16 Narrow - 16 lead Plastic Small Outline, 150 mils body width, Package Outline	42

# 1 Summary description

The CR14 is a contactless coupler that is compliant with the short range ISO14443 type-B standard. It is controlled using the two wire I<sup>2</sup>C bus.

The CR14 generates a 13.56MHz signal on an external antenna. Transmitted data are modulated using Amplitude Shift Keying (ASK). Received data are demodulated from the PICC (Proximity integrated Coupling Card) load variation signal, induced on the antenna, using Bit Phase Shift Keying (BPSK) of a 847kHz sub-carrier. The Transmitted ASK wave is 10% modulated. The Data transfer rate between the CR14 and the PICC is 106 Kbit/s in both transmission and reception modes.

The CR14 follows the ISO14443 type-B recommendation for Radio frequency power and signal interface.

The CR14 is specifically designed for short range applications that need disposable and reusable products.

The CR14 includes an automated anti-collision mechanism that allows it to detect and select any ST short range memories that are present at the same time within its range. The anti-collision mechanism is based on the STMicroelectronics probabilistic scanning method. The CR14 provides a complete analog interface, compliant with the ISO14443 type-B recommendations for Radio-Frequency power and signal interfacing. With it, any ISO14443 type-B PICC products can be powered and have their data transmission controlled via a simple antenna.

The CR14 is fabricated in STMicroelectronics High Endurance Single Poly-silicon CMOS technology.

The CR14 is organized as 4 different blocks (see [Figure 2](#)):

- The I<sup>2</sup>C bus controller. It handles the serial connection with the application host. It is compliant with the 400kHz I<sup>2</sup>C bus specification, and controls the read/write access to all the CR14 registers.
- The RAM buffer. It is bi-directional. . It stores all the request frame Bytes to be transmitted to the PICC, and all the received Bytes sent by the PICC on the answer frame.
- The transmitter. It powers the PICCs by generating a 13.56MHz signal on an external antenna. The resulting field is 10% modulated using ASK (amplitude shift keying) for outgoing data.
- The receiver. It demodulates the signal generated on the antenna by the load variation of the PICC. The resulting signal is decoded by a 847kHz BPSK (binary phase shift keying) sub-carrier decoder.

The CR14 is designed to be connected to a digital host (Microcontroller or ASIC). This host has to manage the entire communication protocol in both transmit and receive modes, through the I<sup>2</sup>C serial bus.

Figure 1. Logic Diagram

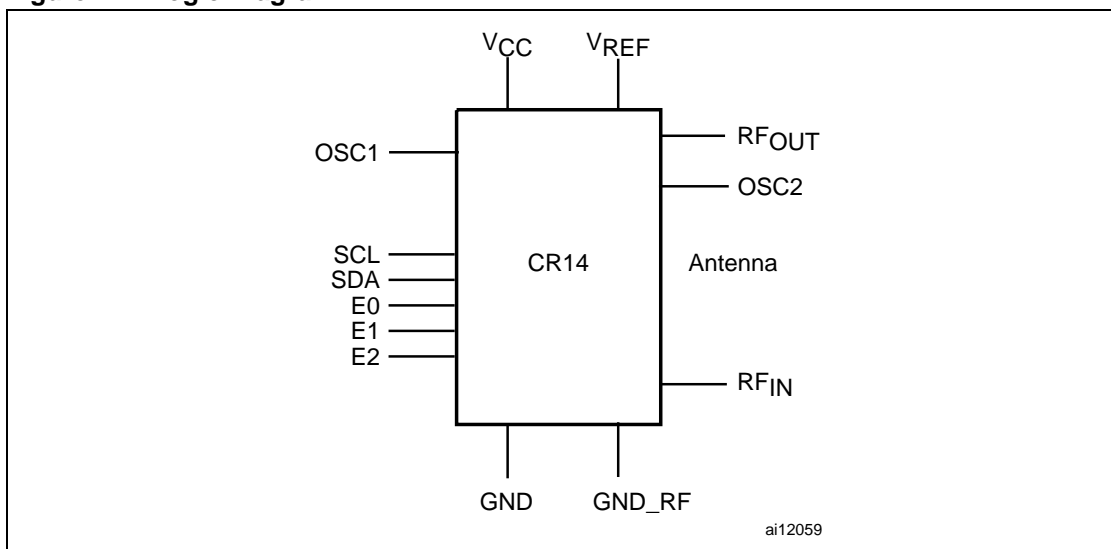
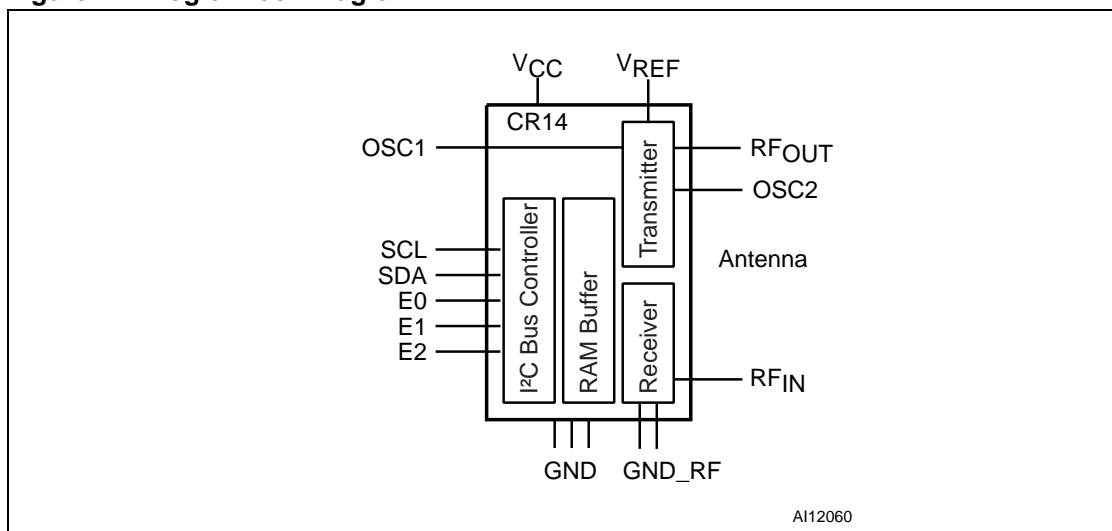


Table 1. Signal Names

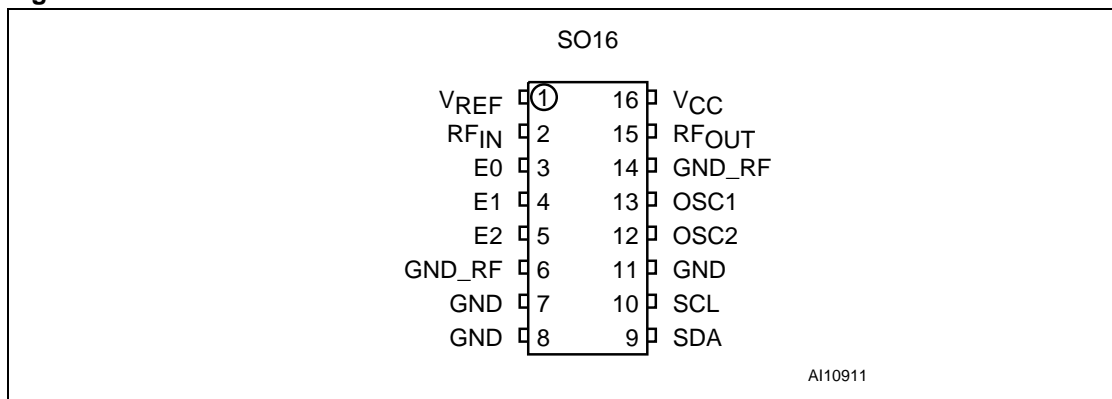
RF <sub>OUT</sub>	Antenna Output Driver
RF <sub>IN</sub>	Antenna Input Filter
OSC1	Oscillator Input
OSC2	Oscillator Output
E0, E1, E2	Chip Enable Inputs
SDA	I <sup>2</sup> C Bi-Directional Data
SCL	I <sup>2</sup> C Clock
V <sub>CC</sub>	Power Supply
GND	Ground
V <sub>REF</sub>	Transmitter Reference Voltage
GND_RF	Ground for RF circuitry

**Figure 2. Logic Block Diagram**



AI12060

**Figure 3. SO Pin Connections**



AI10911



## 2 Signal description

See [Figure 1: Logic Diagram](#), and [Table 1: Signal Names](#), for an overview of the signals connected to this device.

### 2.1 Oscillator (OSC1, OSC2)

The OSC1 and OSC2 pins are internally connected to the on-chip oscillator circuit. The OSC1 pin is the input pin, the OSC2 is the output pin. For correct operation of the CR14, it is required to connect a 13.56MHz quartz crystal across OSC1 and OSC2. If an external clock is used, it must be connected to OSC1 and OSC2 must be left open.

### 2.2 Antenna Output Driver (RF<sub>OUT</sub>)

The Antenna Output Driver pin, RF<sub>OUT</sub>, generates the modulated 13.56MHz signal on the antenna. Care must be taken as it will not withstand a short-circuit.

RF<sub>OUT</sub> has to be connected to the antenna circuitry as shown in [Figure 4: CR14 Application Schematic](#). The LRC antenna circuitry must be connected across the RF<sub>OUT</sub> pin and GND.

### 2.3 Antenna Input Filter (RF<sub>IN</sub>)

The antenna input filter of the CR14, RF<sub>IN</sub>, has to be connected to the external antenna through an adapter circuit, as shown in [Figure 4](#).

The input filter demodulates the signal generated on the antenna by the load variation of the PICC. The resulting signal is then decoded by the 847kHz BPSK decoder.

### 2.4 Transmitter Reference Voltage (V<sub>REF</sub>)

The Transmitter Reference Voltage input, V<sub>REF</sub>, provides a reference voltage used by the output driver for ASK modulation.

The Transmitter Reference Voltage input should be connected to an external capacitor, as shown in [Figure 4](#).

### 2.5 Serial Clock (SCL)

The SCL input pin is used to strobe all I<sup>2</sup>C data in and out of the CR14. In applications where this line is used by slave devices to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the Serial Clock (SCL) to V<sub>CC</sub>. ([Figure 5](#) indicates how the value of the pull-up resistor can be calculated).

In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

## 2.6 Serial Data (SDA)

The SDA signal is bi-directional. It is used to transfer I<sup>2</sup>C data in and out of the CR14. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial data (SDA) to V<sub>CC</sub>. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

## 2.7 Chip Enable (E0, E1, E2)

The Chip Enable inputs E0, E1, E2 are used to set and reset the value on the three least significant bits (b3, b2, b1) of the 7-bit I<sup>2</sup>C Device Select Code. They are used for hardwired addressing, allowing up to eight CR14 devices to be addressed on the same I<sup>2</sup>C bus. These inputs may be driven dynamically or tied to V<sub>CC</sub> or GND to establish the Device Select Code (note that the V<sub>IL</sub> and V<sub>IH</sub> levels for the inputs are CMOS compatible, not TTL compatible).

When left open, E0, E1 and E2 are internally read at the logic level 0 due to the internal pull-down resistors connected to each inputs.

## 2.8 Power Supply (V<sub>CC</sub>, GND, GND\_RF)

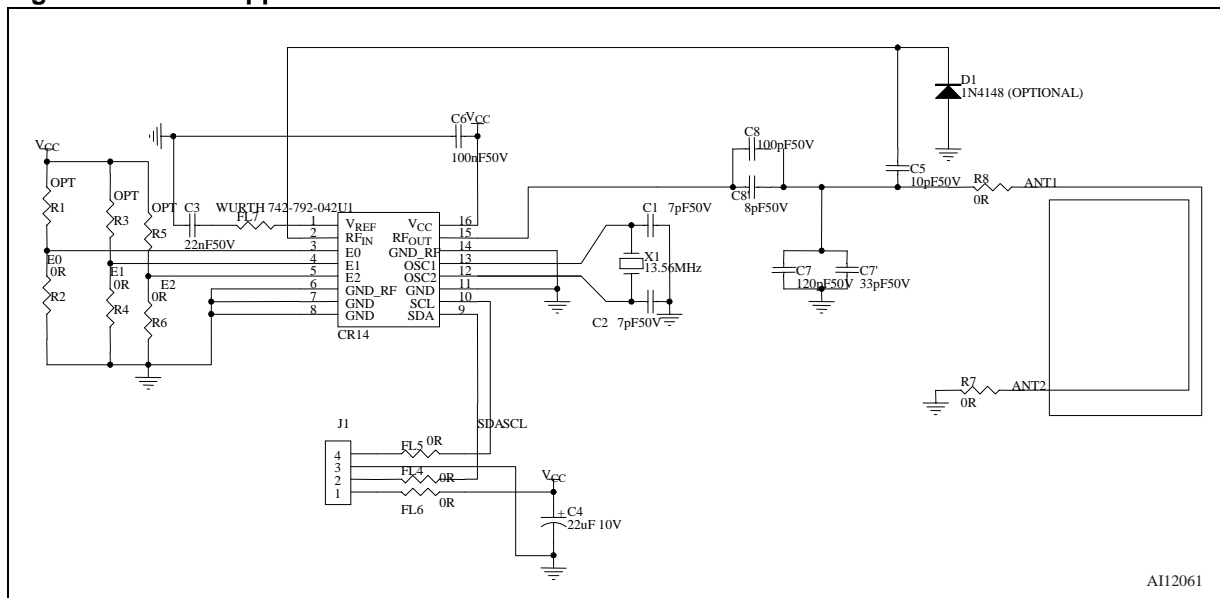
Power is supplied to the CR14 using the V<sub>CC</sub>, GND and GND\_RF pins.

V<sub>CC</sub> is the Power Supply pin that supplies the power (+5V) for all CR14 operations.

The GND and GND\_RF pins are ground connections. They must be connected together.

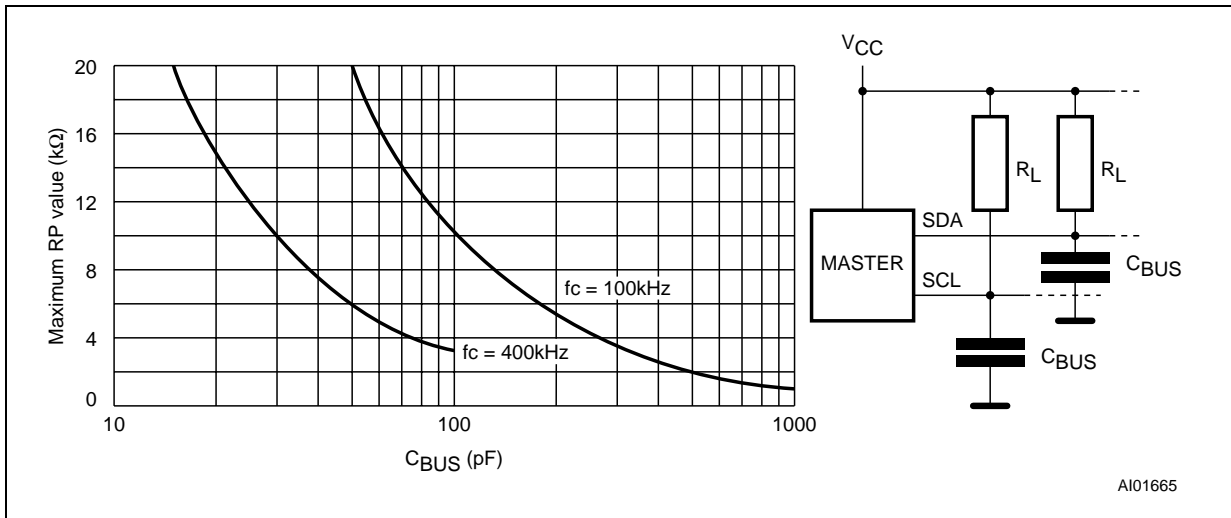
Decoupling capacitors should be connected between the V<sub>CC</sub> Supply Voltage pin, the GND Ground pin and the GND\_REF Ground pin to filter the power line, as shown in *Figure 4*.

Figure 4. CR14 Application Schematic



AI12061

Figure 5. Maximum  $R_L$  Value versus Bus Capacitance ( $C_{BUS}$ ) for an I<sup>2</sup>C Bus



### 3 CR14 registers

The CR14 chip coupler contains six volatile registers. It is entirely controlled, at both digital and analog level, using the three registers listed below and shown in [Table 2](#):

- Parameter Register
- Input/Output Frame Register
- Slot Marker Register

The other 3 registers are located at addresses 02h, 04h and 05h. They are “ST Reserved”, and must not be used in end-user applications.

In the I<sup>2</sup>C protocol, all data Bytes are transmitted Most Significant Byte first, with each Byte transmitted Most significant bit first.

**Table 2. CR14 Control Registers**

Address		Length	Access	Purpose
00h	Parameter Register	1 Byte	W	Set parameter register
			R	Read parameter register
01h	Input/output Frame Register	36 Bytes	W	Store and send request frame to the PICC. Wait for PICC answer frame
			R	Transfer PICC answered frame data to Host
02h	ST Reserved	NA	W	ST Reserved, must not be used.
			R	
03h	Slot Marker Register	1 Byte	W	Launch the automated anti-collision process from Slot_0 to Slot_15
			R	Return data FFh
04h	ST Reserved	NA	R and W	ST Reserved. Must not be used
05h	ST Reserved	NA	R and W	ST Reserved. Must not be used

### 3.1 Parameter Register (00h)

The Parameter Register is an 8-bit volatile register used to configure the CR14, and thus, to customize the circuit behavior. The Parameter Register is located at the I<sup>2</sup>C address 00h and it is accessible in I<sup>2</sup>C Read and Write modes. Its default value, 00h, puts the CR14 in standard ISO14443 type-B configuration.

**Table 3. Parameter Register Bits Description**

Bit	Control	Value	Description
b <sub>0</sub>	Frame Standard	0	ISO14443 type-B frame management
		1	RFU <sup>(1)</sup>
b <sub>1</sub>	RFU	0	Not used
b <sub>2</sub>	Answer Frame Format	0	Answer PICC Frames are delimited by SOF and EOF
		1	Answer PICC Frames do not provide SOF and EOF delimiters
b <sub>3</sub>	ASK Modulation Depth	0	10% ASK modulation depth mode
		1	RFU
b <sub>4</sub>	Carrier Frequency	0	13.56MHz carrier on RF OUT is OFF
		1	13.56MHz carrier on RF OUT is ON
b <sub>5</sub>	t <sub>WDG</sub> Answer delay watchdog	b5=0, b6=0: Watchdog time-out = 500μs to be used for read	
b <sub>6</sub>		b5=0, b6=1: Watchdog time-out = 5ms to be used for read	
		b5=1, b6=0: Watchdog time-out = 10ms to be used for write	
		b5=1, b6=1: Watchdog time-out = 309ms to be used for MCU timings	
b <sub>7</sub>	RFU	0	Not used

1. RFU = Reserved for Future Use.

### 3.2 Input/Output Frame Register (01h)

The Input/Output Frame Register is a 36-Byte buffer that is accessed serially from Byte 0 through to Byte 35 (see [Table 4](#)). It is located at the I<sup>2</sup>C address 01h.

The Input/Output Frame Register is the buffer in which the CR14 stores the data Bytes of the request frame to be sent to the PICC. It automatically stores the data Bytes of the answer frame received from the PICC. The first Byte (Byte 0) of the Input/Output Frame Register is used to store the frame length for both transmission and reception.

When accessed in I<sup>2</sup>C Write mode, the register stores the request frame Bytes that are to be transmitted to the PICC. Byte 0 must be set with the request frame length (in Bytes) and the frame is stored from Byte 1 onwards. At the end of the transmission, the 16-bit CRC is automatically added. After the transmission, the CR14 wait for the PICC to send back an answer frame. When correctly decoded, the PICC answer frame Bytes are stored in the Input/Output Frame Register from Byte 1 onwards. Byte 0 stores the number of Bytes received from the PICC.

When accessed in I<sup>2</sup>C Read mode, the Input/Output Register sends back the last PICC answer frame Bytes, if any, with Byte 0 transmitted first. The 16-bit CRC is not stored, and it is not sent back on the I<sup>2</sup>C bus.

The Input/Output Frame Register is set to all 00h between transmission and reception. If there is no answer from the PICC, Byte 0 is set to 00h. In the case of a CRC error, Byte 0 is set to FFh, and the data Bytes are discarded and not appended in the register.

The CR14 Input/Output Frame Register is so designed as to generate all the ST short range memory command frames. It can also generate all standardized ISO14443 type-B command frames like REQB, SLOT-MARKER, ATTRIB, HALT, and get all the answers like ATQB, or answer to ATTRIB. All ISO14443 type-B compliant PICCs can be accessed by the CR14 provided that their data frame exchange is not longer than 35 Bytes in both request and answer.

**Table 4. Input/Output Frame Register Description**

Byte 0	Byte 1	Byte 2	Byte 3	...	Byte 34	Byte 35
Frame Length	First data Byte	Second data Byte				Last data Byte
<----- Request and Answer Frame Bytes exchanged on the RF ----->						
00h No Byte transmitted						
FFh CRC Error						
xxh Number of transmitted Bytes						

### 3.3 Slot Marker Register (03h)

The slot Marker Register is located at the I<sup>2</sup>C address 03h. It is used to trigger an automated anti-collision sequence between the CR14 and any ST short range memory present in the electromagnetic field. With one I<sup>2</sup>C access, the CR14 launches a complete stream of commands starting from PCALL16(), SLOT\_MARKER(1), SLOT\_MARKER(2) up to SLOT\_MARKER(15), and stores all the identified Chip\_IDs into the Input/Output Frame Register (I<sup>2</sup>C address 01h).

This automated anti-collision sequence simplifies the host software development and reduces the time needed to interrogate the 16 slots of the STMicroelectronics anti-collision mechanism.

When accessed in I<sup>2</sup>C Write mode, the Slot Marker Register starts generating the sequence of anti-collision commands. After each command, the CR14 wait for the ST short range memory answer frame which contains the Chip\_ID. The validity of the answer is checked and stored into the corresponding Status Slot Bit (Byte 1 and Byte 2 as described in [Table 6](#)). If the answer is correct, the Status Slot Bit is set to '1' and the Chip\_ID is stored into the corresponding Slot\_Register. If no answer is detected, the Status Slot Bit is set to '0', and the corresponding Slot\_Register is set to 00h. If a CRC error is detected, the Status Slot Bit is set to '0', and the corresponding Slot\_Register is set to FFh.

Each time the Slot Marker Register is accessed in I<sup>2</sup>C Write mode, Byte 0 of the Input/Output Frame Register is set to 18, Bytes 1 and 2 provide Status Bits Slot information, and Bytes 3 to 18 store the corresponding Chip\_ID or error code.

The Slot Marker Register cannot be accessed in I<sup>2</sup>C Read mode. All the anti-collision data can be accessed by reading the Input/Output Frame Register at the I<sup>2</sup>C address 01h.

**Table 5. Slot Marker Register Description**

	b <sub>7</sub>	b <sub>6</sub>	b <sub>5</sub>	b <sub>4</sub>	b <sub>3</sub>	b <sub>2</sub>	b <sub>1</sub>	b <sub>0</sub>
Byte 0	Number of stored Bytes: fixed to 18							
Byte 1	Status Slot Bit 7	Status Slot Bit 6	Status Slot Bit 5	Status Slot Bit 4	Status Slot Bit 3	Status Slot Bit 2	Status Slot Bit 1	Status Slot Bit 0
Byte 2	Status Slot Bit 15	Status Slot Bit 14	Status Slot Bit 13	Status Slot Bit 12	Status Slot Bit 11	Status Slot Bit 10	Status Slot Bit 9	Status Slot Bit 8
Byte 3	Slot_Register 0 = Chip_ID value detected in Slot 0							
Byte 4	Slot_Register 1 = Chip_ID value detected in Slot 1							
Byte 5	Slot_Register 2 = Chip_ID value detected in Slot 2							
Byte 6	Slot_Register 3 = Chip_ID value detected in Slot 3							
Byte n	.....							
Byte 17	Slot_Register 14 = Chip_ID value detected in Slot 14							
Byte 18	Slot_Register 15 = Chip_ID value detected in Slot 15							

Status bit value description:

1: No error detected. The Chip\_ID stored in the Slot register is valid.

0: Error detected

– Slot register = 00h: No answer frame detected from ST short range memory

– Slot register = FFh: Answer Frame detected with CRC error. Collision may have occurred

## 4 CR14 I<sup>2</sup>C protocol description

The CR14 is compatible with the I<sup>2</sup>C serial bus memory standard, which is a two-wire serial interface that uses a bi-directional data bus and serial clock.

The CR14 has a pre-programmed, 4-bit identification code, '1010' (as shown in [Table 6](#)), that corresponds to the I<sup>2</sup>C bus definition. With this code and the three Chip Enable inputs (E2, E1, E0) up to eight CR14 devices can be connected to the I<sup>2</sup>C bus, and selected individually.

The CR14 behaves as a slave device in the I<sup>2</sup>C protocol, with all CR14 operations synchronized to the serial clock.

I<sup>2</sup>C Read and Write operations are initiated by a START condition, generated by the bus master.

The START condition is followed by the Device Select Code and by a Read/Write bit ( $\overline{RW}$ ). It is terminated by an acknowledge bit. The Device Select Code consists of seven bits (as shown in [Table 6](#)):

- the Device Code (first four bits)
- plus three bits corresponding to the states of the three Chip Enable inputs, E2, E1 and E0, respectively

When data is written to the CR14, the device inserts an acknowledge bit (9th bit) after the bus master's 8-bit transmission.

When the bus master reads data, it also acknowledges the receipt of the data Byte by inserting an acknowledge bit (9th bit).

Data transfers are terminated by a STOP condition after an ACK for Write, or after a NoACK for Read.

The CR14 supports the I<sup>2</sup>C protocol, as summarized in [Figure 6](#).

Any device that sends data on to the bus, is defined as a transmitter, and any device that reads the data, as a receiver.

The device that controls the data transfer is known as the master, and the other, as the slave. A data transfer can only be initiated by the master, which also provides the serial clock for synchronization. The CR14 is always a slave device in all I<sup>2</sup>C communications. All data are transmitted Most Significant Bit (MSB) first.

**Table 6. Device Select Code**

	Device Code				Chip Enable			R $\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
CR14 Select	1	0	1	0	E2	E1	E0	R $\overline{W}$



## 4.1 I<sup>2</sup>C Start Condition

START is identified by a High-to-Low transition of the Serial Data line, SDA, while the Serial Clock, SCL, is stable in the High state. A START condition must precede any data transfer command.

The CR14 continuously monitors the SDA and SCL lines for a START condition (except during Radio Frequency data exchanges), and will not respond unless one is sent.

## 4.2 I<sup>2</sup>C Stop Condition

STOP is identified by a Low-to-High transition of the Serial Data line, SDA, while the Serial Clock, SCL, is stable in the High state.

A STOP condition terminates communications between the CR14 and the bus master.

A STOP condition at the end of an I<sup>2</sup>C Read command, after (and only after) a NoACK, forces the CR14 into its stand-by state.

A STOP condition at the end of an I<sup>2</sup>C Write command triggers the Radio Frequency data exchange between the CR14 and the PICC.

## 4.3 I<sup>2</sup>C Acknowledge Bit (ACK)

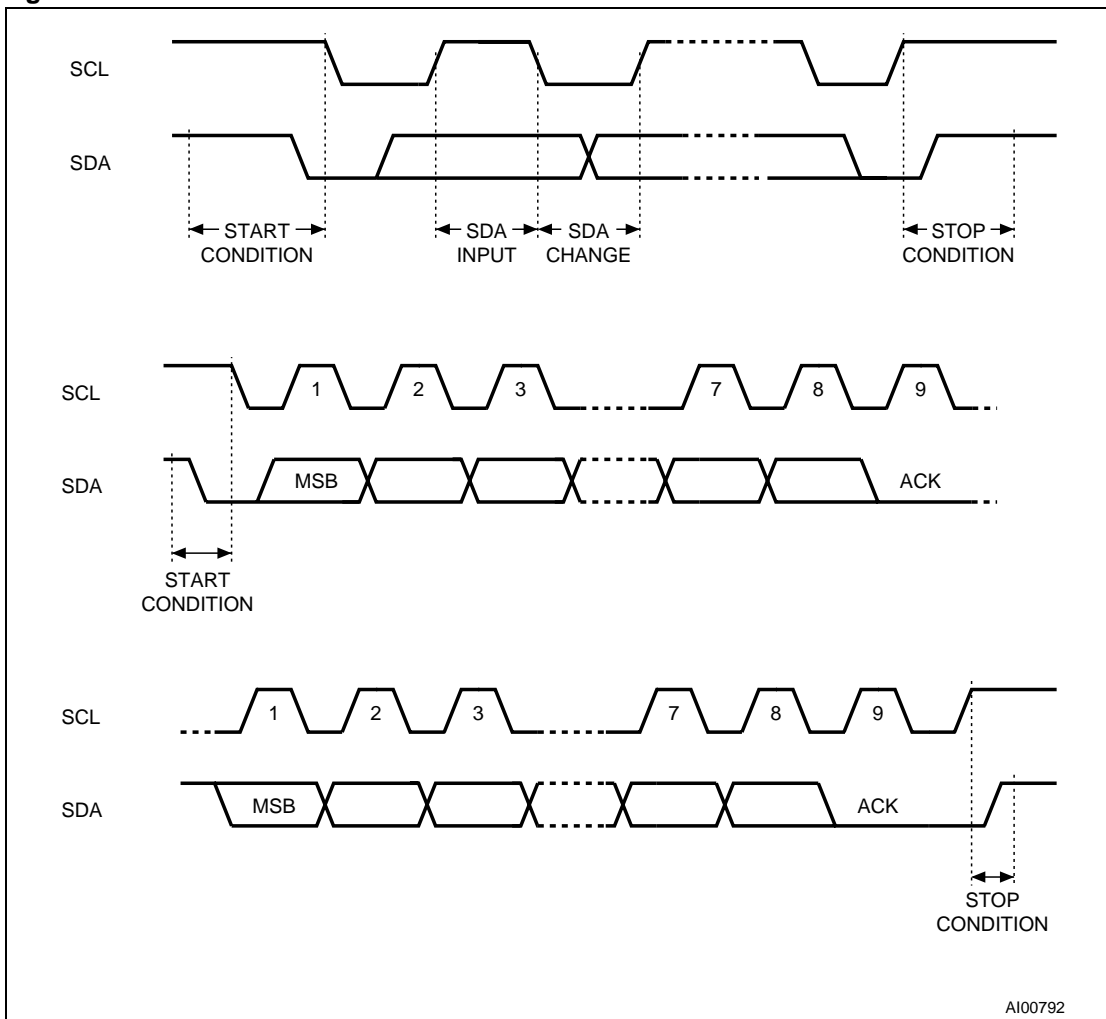
An acknowledge bit is used to indicate a successful data transfer on the I<sup>2</sup>C bus.

The bus transmitter, either master or slave, releases the Serial Data line, SDA, after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA line Low to acknowledge the receipt of the 8 data bits.

## 4.4 I<sup>2</sup>C Data Input

During data input, the CR14 samples the SDA bus signal on the rising edge of the Serial Clock, SCL. For correct device operation, the SDA signal must be stable during the Low-to-High Serial Clock transition, and the data must change only when the SCL line is Low

**Figure 6. I<sup>2</sup>C Bus Protocol**



### 4.5 I<sup>2</sup>C Memory Addressing

To start up communication with the CR14, the bus master must initiate a START condition. Then, the bus master sends 8 bits (with the most significant bit first) on the Serial Data line, SDA. These bits consist of the Device Select Code (7 bits) plus a  $\overline{RW}$  bit.

According to the I<sup>2</sup>C bus definition, the seven most significant bits of the Device Select Code are the Device Type Identifier. For the CR14, these bits are defined as shown in [Table 6](#).

The 8th bit is the Read/Write bit ( $\overline{RW}$ ). It is set to '1' for I<sup>2</sup>C Read, and to '0' for I<sup>2</sup>C Write operations.

If the data sent by the bus master matches the Device Select Code of a CR14 device, the corresponding device returns an acknowledgment on the SDA bus during the 9<sup>th</sup> bit time.

The CR14 devices whose Device Select Codes do not correspond to the data sent, generate a No-ACK. They deselect themselves from the bus and go into stand-by mode.

## 4.6 CR14 I<sup>2</sup>C Write Operations

The bus master sends a START condition, followed by a Device Select Code and the R/W bit set to '0'. The CR14 that corresponds to the Device Select Code, acknowledges and waits for the bus master to send the Byte address of the register that is to be written to. After receipt of the address, the CR14 returns another ACK, and waits for the bus master to send the data Bytes that are to be written.

In the CR14 I<sup>2</sup>C Write mode, the bus master may send one or more data Bytes depending on the selected register.

The CR14 replies with an ACK after each data Byte received. The bus master terminates the transfer by generating a STOP condition.

The STOP condition at the end of a Write access to the Input/Output Frame Register causes the Radio Frequency data exchange between the CR14 and the PICC to be started.

During the Radio Frequency data exchange, the CR14 disconnects itself from the I<sup>2</sup>C bus. The time ( $t_{RFEX}$ ) needed to complete the exchange is not fixed as it depends on the PICC command format. To know when the exchange is complete, the bus master uses an ACK polling sequence as shown in [Figure 8](#). It consists of the following:

- Initial condition: a Radio Frequency data exchange is in progress.
- Step 1: the master issues a START condition followed by the first Byte of the new instruction (Device Select Code plus R/W bit).
- Step 2: if the CR14 is busy, no ACK is returned and the master goes back to Step 1. If the CR14 has completed the Radio Frequency data exchange, it responds with an ACK, indicating that it is ready to receive the second part of the next instruction (the first Byte of this instruction being sent during Step 1).

**Figure 7. CR14 I<sup>2</sup>C Write Mode Sequence**

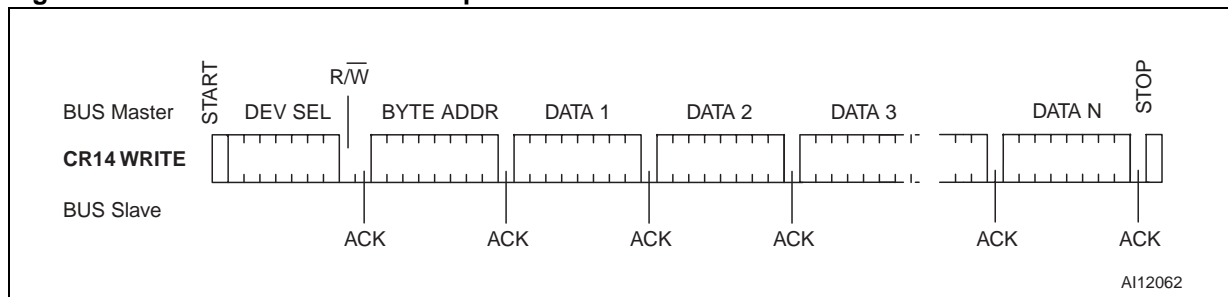
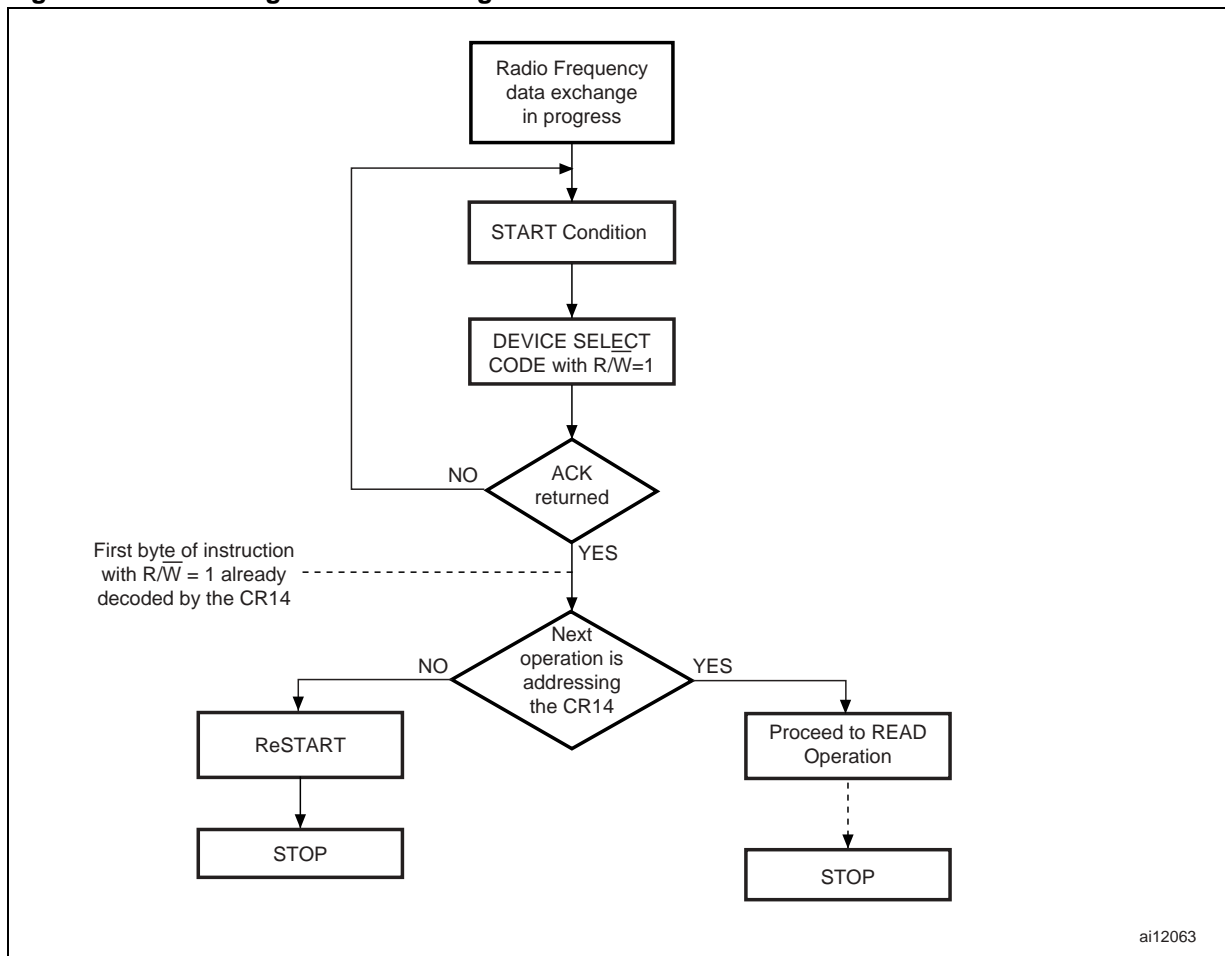


Figure 8. I<sup>2</sup>C Polling Flowchart using ACK



## 4.7 CR14 I<sup>2</sup>C Read Operations

To send a Read command, the bus master sends a START condition, followed by a Device Select Code and the R/W bit set to '1'.

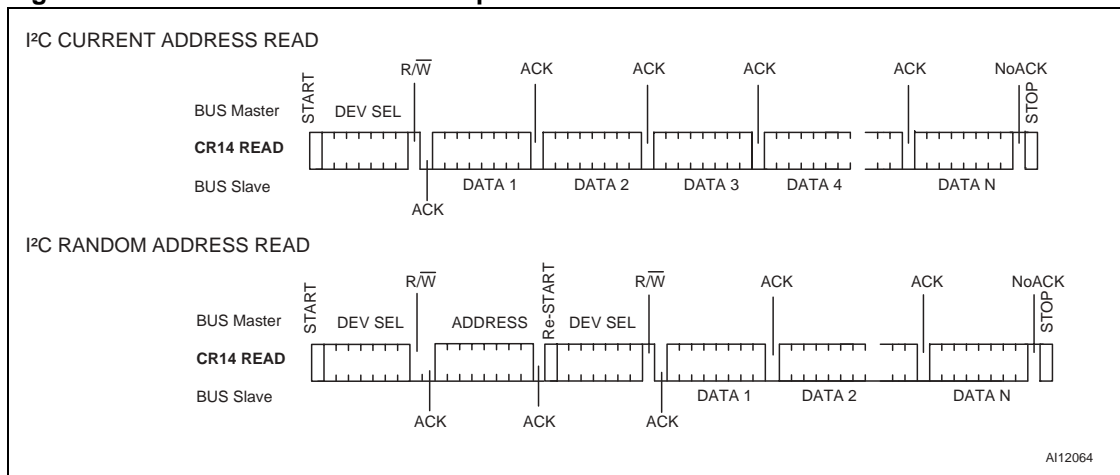
The CR14 that corresponds to the Device Select Code acknowledges and outputs the first data Byte of the addressed register.

To select a specific register, a dummy Write command must first be issued, giving an address Byte but no data Bytes, as shown in the bottom half of *Figure 9*. This causes the new address to be stored in the internal address pointer, for use by the Read command that immediately follows the dummy Write command.

In the I<sup>2</sup>C Read mode, the CR14 may read one or more data Bytes depending on the selected register. The bus master has to generate an ACK after each data Byte to read all the register data in a continuous stream. Only the last data Byte should not be followed by an ACK. The master then terminates the transfer with a STOP condition, as shown in *Figure 9*.

After reading each Byte, the CR14 waits for the master to send an ACK during the 9<sup>th</sup> bit time. If the master does not return an ACK within this time, the CR14 terminates the data transfer and switches to stand-by mode.

**Figure 9. CR14 I<sup>2</sup>C Read Modes Sequences**



## 5 Applying the I<sup>2</sup>C protocol to the CR14 registers

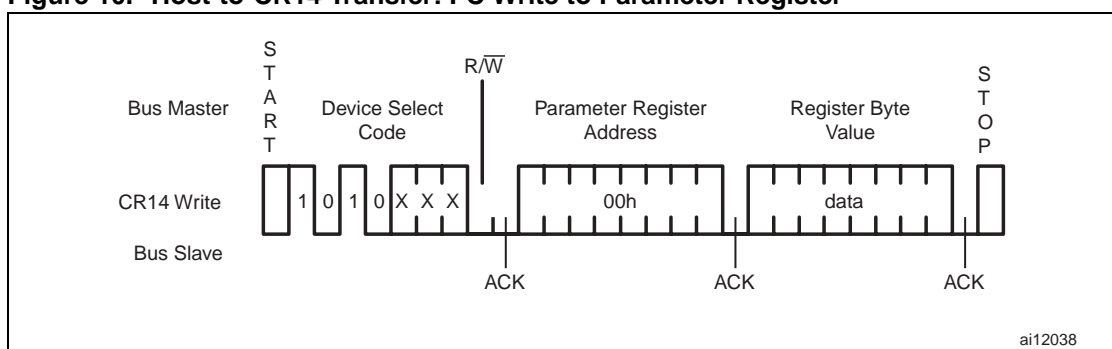
### 5.1 I<sup>2</sup>C Parameter Register Protocol

Figure 10 shows how new data is written to the Parameter Register. The new value becomes active after the I<sup>2</sup>C STOP condition.

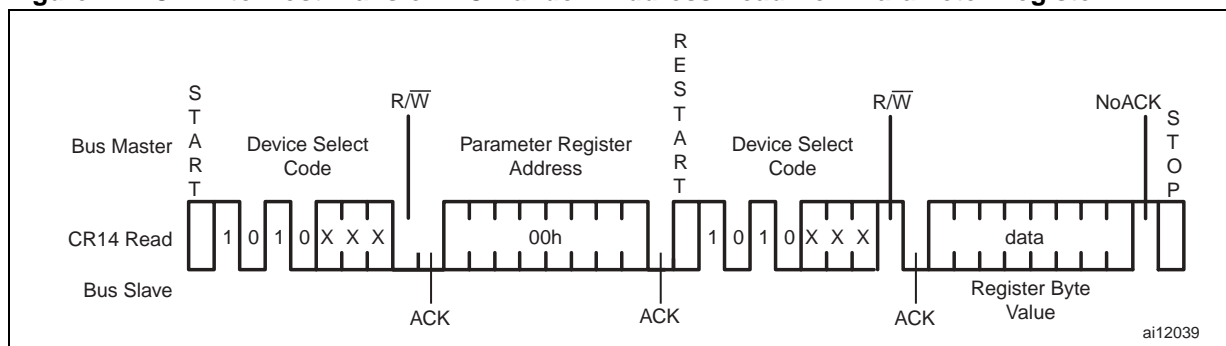
Figure 11 shows how to read the Parameter Register contents. The CR14 sends and re-sends the Parameter Register contents until it receives a NoACK from the I<sup>2</sup>C Host.

The CR14 supports the I<sup>2</sup>C Current Address and Random Address Read modes. The Current Address Read mode can be used if the previous command was issued to the register where the Read is to take place.

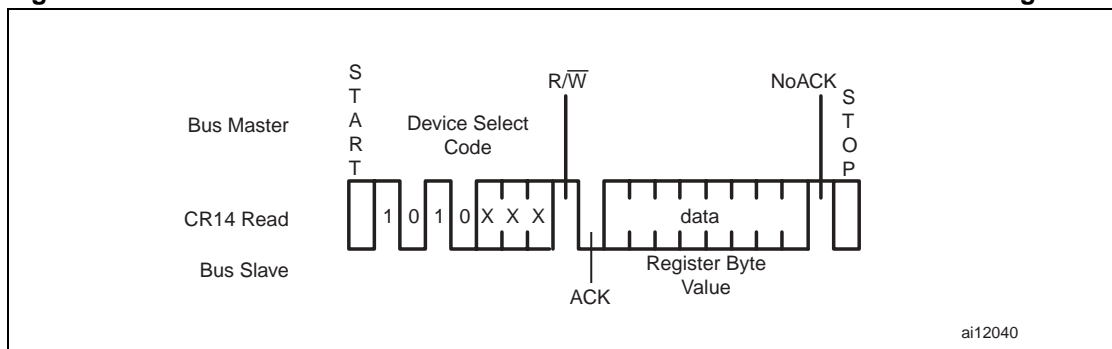
**Figure 10. Host-to-CR14 Transfer: I<sup>2</sup>C Write to Parameter Register**



**Figure 11. CR14-to-Host Transfer: I<sup>2</sup>C Random Address Read from Parameter Register**



**Figure 12. CR14-to-Host Transfer: I<sup>2</sup>C Current Address Read from Parameter Register**



## 5.2 I<sup>2</sup>C Input/Output Frame Register Protocol

Figure 13 shows how to store a PICC request frame command of *N* Bytes into the Input/Output Frame Register.

After the I<sup>2</sup>C STOP condition, the request frame is RF transmitted in the ISO14443 type-B format. The CR14 then waits for the PICC answer frame which will also be stored in the Input/Output Frame Register. The request frame is over-written by the answer frame.

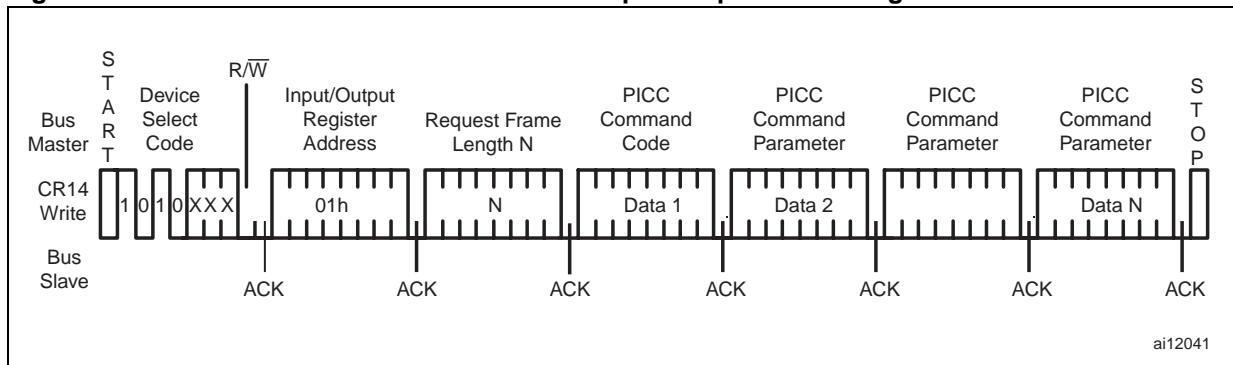
Figure 14 shows how to read an *N*-Byte PICC answer frame.

The two CRC Bytes generated by the PICC are not stored.

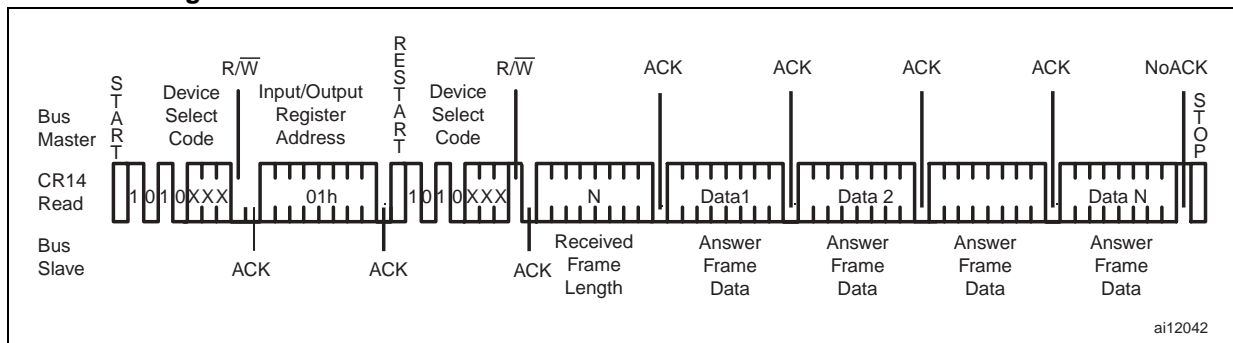
The CR14 continues to output data Bytes until a NoACK has been generated by the I<sup>2</sup>C Host, and received by the CR14. After all 36 Bytes have been output, the CR14 “rolls over”, and starts outputting from the start of the Input/Output Frame Register again.

The CR14 supports the I<sup>2</sup>C Current Address and Random Address Read modes. The Current Address Read mode can be used if the previous command was issued to the register where the Read is to take place.

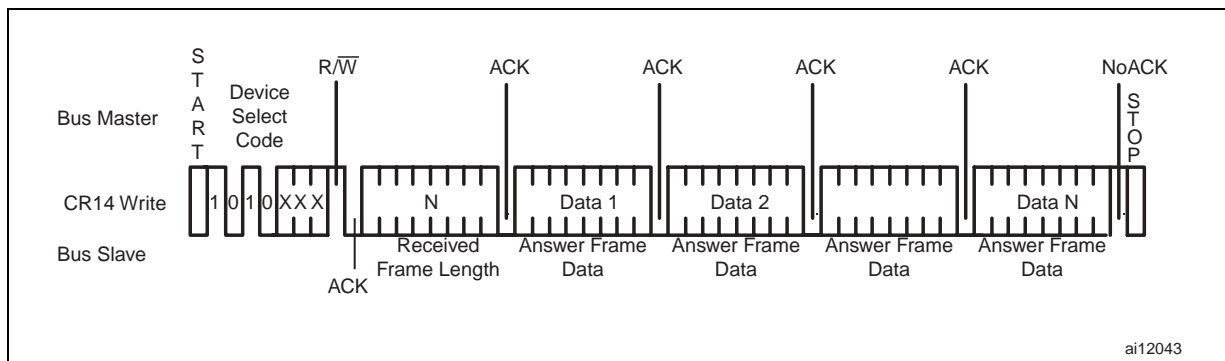
**Figure 13. Host-to-CR14 Transfer: I<sup>2</sup>C Write to Input/Output Frame Register for ISO14443B**



**Figure 14. CR14-to-Host Transfer: I<sup>2</sup>C Random Address Read from Input/Output Frame Register for ISO14443B**



**Figure 15. CR14-to-Host Transfer: I<sup>2</sup>C Current Address Read from I/O Frame Register for ISO14443B**



### 5.3 I<sup>2</sup>C Slot Marker Register Protocol

An I<sup>2</sup>C Write command to the Slot Marker Register generates an automated sixteen-command loop (See [Figure 16](#) for a description of the command).

All the answers from the ST short range memory devices that are detected, are written in the Input/Output Frame Register.

Read from the I<sup>2</sup>C Slot Marker Register is not supported by the CR14. If the I<sup>2</sup>C Host tries to read the Slot Marker Register, the CR14 will return the data value FFh in both Random Address and Current Address Read modes until NoACK is generated by the I<sup>2</sup>C Host.

The result of the detection sequence is stored in the Input/Output Frame Register. This Register can be read by the host by using I<sup>2</sup>C Random Address Read.

**Figure 16. Host-to-CR14 Transfer: I<sup>2</sup>C Write to Slot Marker Register**

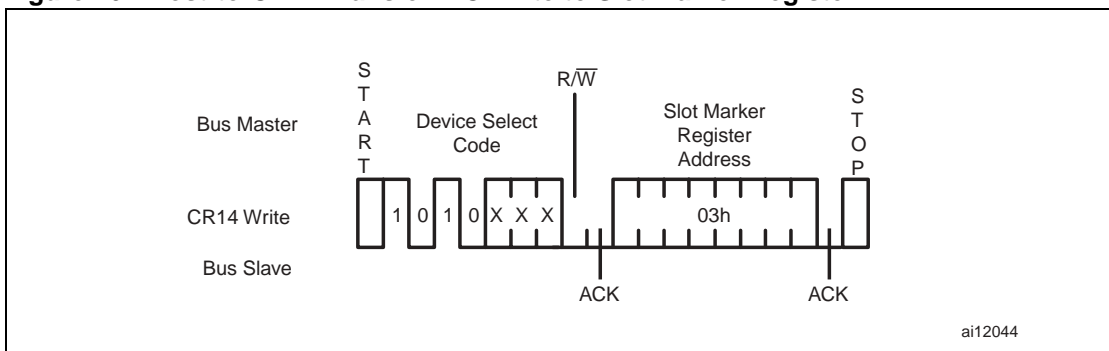




Figure 17. CR14-to-Host Transfer: I<sup>2</sup>C Random Address Read from Slot Marker Register

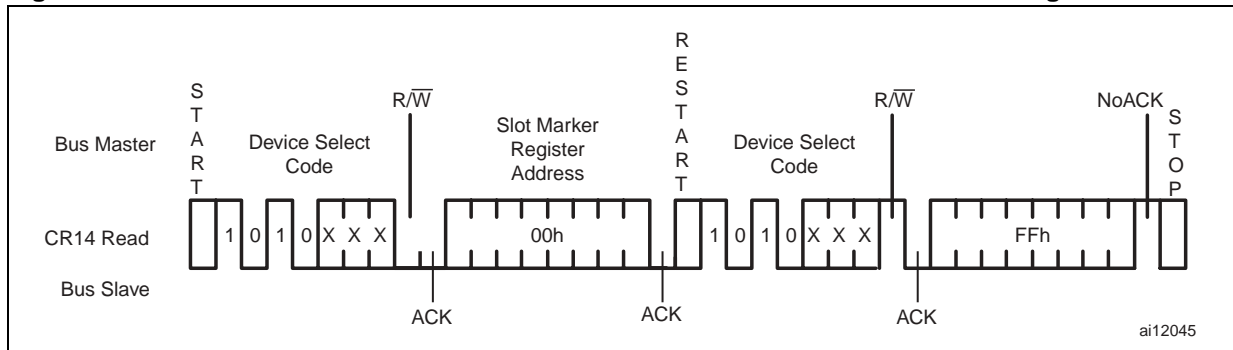
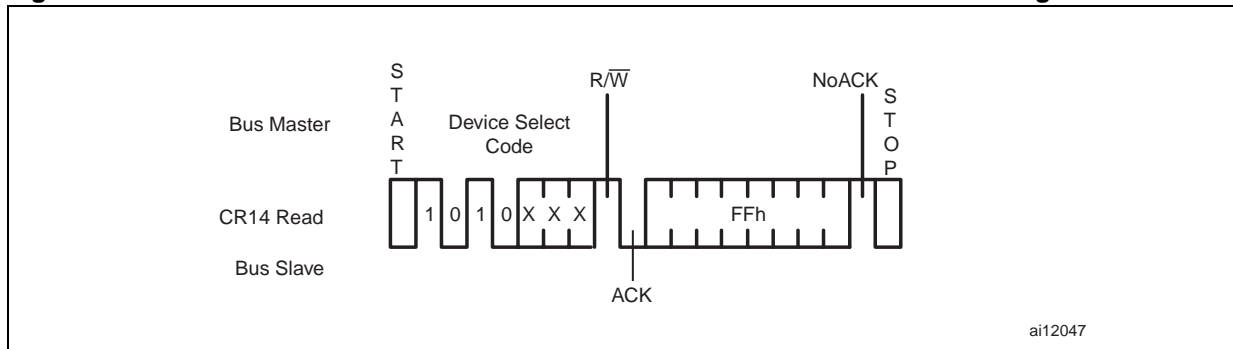


Figure 18. CR14-to-Host Transfer: I<sup>2</sup>C Current Address Read from Slot Marker Register



## 5.4 Addresses above Location 06h

In I<sup>2</sup>C Write mode, when the CR14 receives the 8-bit register address, and the address is above location 06h, the device does not acknowledge (NoACK) and deselects itself from the bus. The Serial Data line, SDA, stays at logic '1' (pull-up resistor), and the I<sup>2</sup>C Host receives a NoACK during the 9th bit time. The SDA line stays High until the STOP condition is issued.

In the I<sup>2</sup>C Current and Random Address Read modes, when the CR14 receives the 8-bit register address, and the address is above location 06h, the device does not acknowledge the Device Select Code after the START condition, and deselects itself from the bus.

## 6 CR14 ISO14443 type-B Radio Frequency data transfer

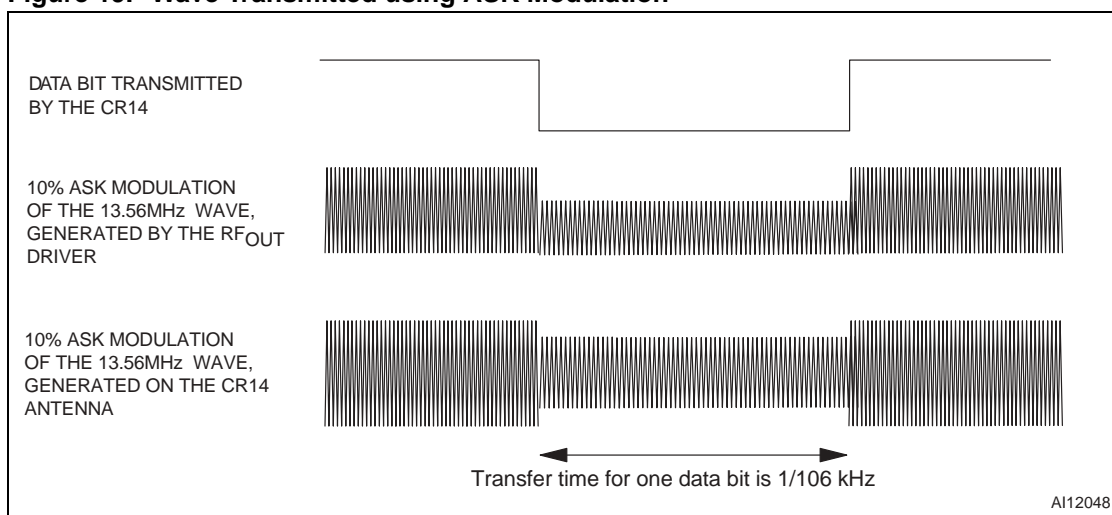
### 6.1 Output RF Data Transfer from the CR14 to the PICC (Request Frame)

The CR14 output buffer is controlled by the 13.56MHz clock signal generated by the external oscillator and by the request frame generator. The CR14 can be directly connected to an external matching circuit to generate a 13.56MHz sinusoidal carrier frequency on its antenna.

The current driven into the antenna coil is directly generated by the CR14 RFOUT output driver.

If the antenna is correctly tuned, it emits an H-field of a large enough magnitude to power a contactless PICC from a short distance. The energy received on the PICC antenna is converted to a Power Supply Voltage by a regulator, and turned into data bits by the ASK demodulator. The CR14 amplitude modulates the 13.56MHz wave by 10% as represented in *Figure 19*. The data transfer rate is 106 kbit/s.

**Figure 19. Wave Transmitted using ASK Modulation**



## 6.2 Transmission Format of Request Frame Characters

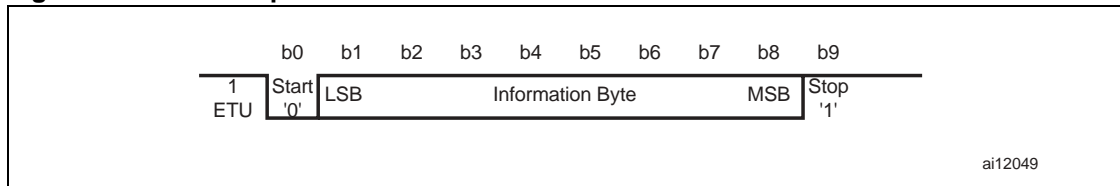
The CR14 transmits characters of 10 bits, with the Least Significant Bit ( $b_0$ ) transmitted first, as shown in [Figure 20](#).

Several 10-bit characters, preceded by the Start Of Frame (SOF) and followed by the End Of Frame (EOF), constitute a Request Frame, as shown in [Figure 26](#).

A Request Frame includes the SOF, instructions, addresses, data, CRC and the EOF as defined in the ISO14443 type-B.

Each bit duration is called an Elementary Time Unit (ETU). One ETU is equal to  $9.44\mu\text{s}$  ( $1/106\text{kHz}$ ).

**Figure 20. CR14 Request Frame Character Format**



**Table 7. CR14 Request Frame Character Format**

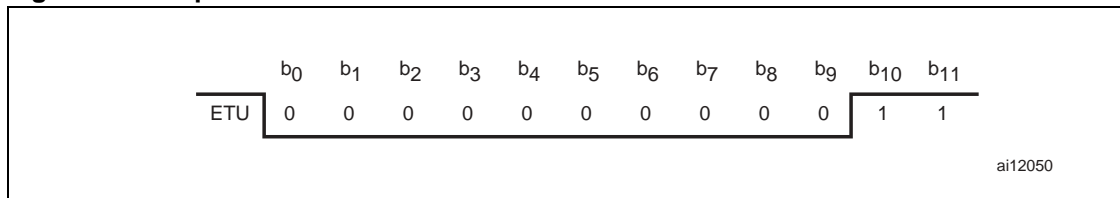
Bit	Description	Value
$b_0$	Start bit used to synchronize the transmission	$b_0 = 0$
$b_1$ to $b_8$	Information Byte (instruction, address or data)	Information Byte is sent Least Significant Bit first
$b_9$	Stop bit used to indicate the end of the character	$b_9 = 1$

## 6.3 Request Start Of Frame

The Start Of Frame (SOF) described in [Figure 21](#) consists of:

- a falling edge,
- followed by ten Elementary Time Units (ETU) each containing a logical '0'
- followed by a single rising edge
- followed by two ETUs, each containing a logical '1'.

**Figure 21. Request Start Of Frame**

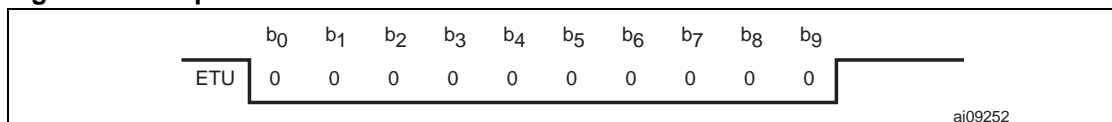


### 6.4 Request End Of Frame

The End Of Frame (EOF) shown in *Figure 22* consists of:

- a falling edge,
- followed by ten Elementary Time Units (ETU) containing each a logical '0',
- followed by a single rising edge.

**Figure 22. Request End Of Frame**



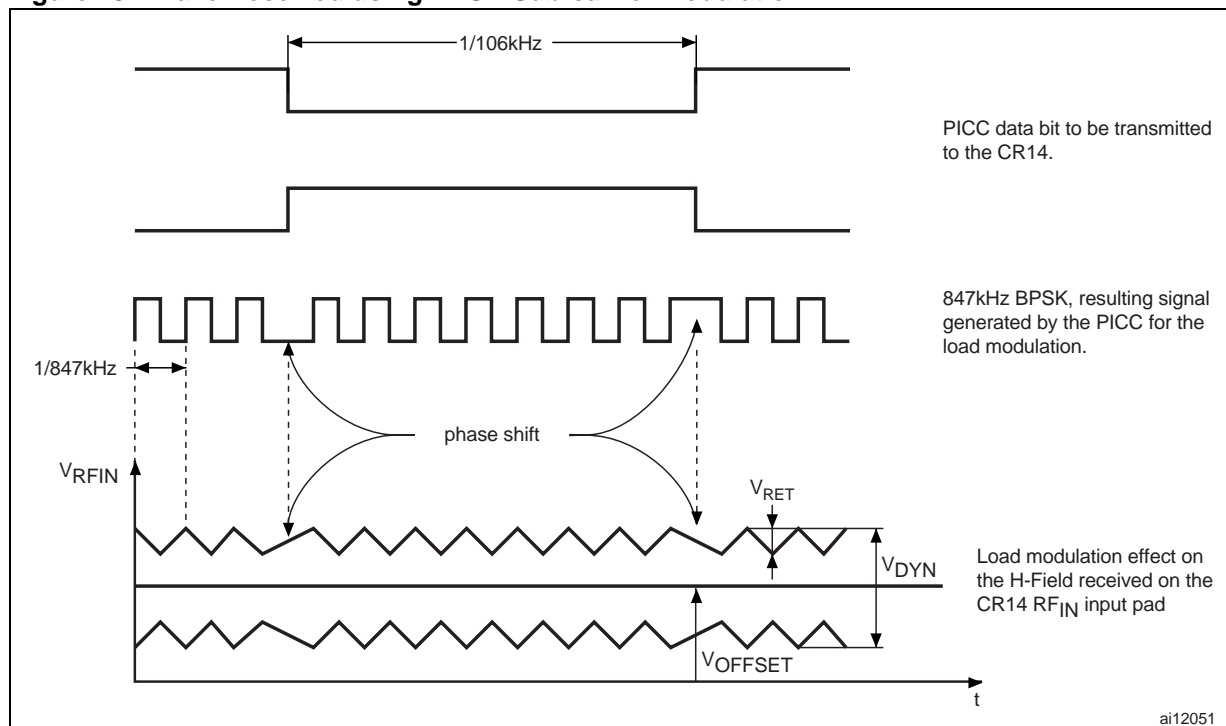
### 6.5 Input RF Data Transfer from the PICC to the CR14 (Answer Frame)

The CR14 uses the ISO14443 type-B retro-modulation scheme which is demodulated and decoded by the RF<sub>IN</sub> circuitry.

The modulation is obtained by modifying the PICC current consumption (load modulation). This load modulation induces an H-field variation, by coupling, that is detected by the CR14 RF<sub>IN</sub> input as a voltage variation on the antenna. The RF<sub>IN</sub> input demodulates this variation and decodes the information received from the PICC.

Data must be transmitted using a 847kHz, BPSK modulated sub-carrier frequency, f<sub>S</sub>, as shown in *Figure 23*, and as specified in ISO14443 type-B. In BPSK, all data state transitions (from '0' to '1' or from '1' to '0') are encoded by phase shift keying the sub-carrier.

**Figure 23. Wave Received using BPSK Sub-carrier Modulation**



## 6.6 Transmission Format of Answer Frame Characters

The PICC should use the same character format as that used for output data transfer (see [Figure 20](#)).

An Answer Frame includes the SOF, data, CRC and the EOF, as illustrated in [Figure 26](#). The data transfer rate is 106 kbit/s.

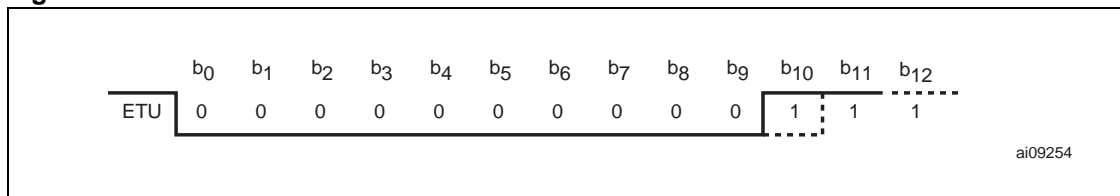
The CR14 will also accept Answer Frames that do not contain the SOF and EOF delimiters, provided that these Frames are correctly set in the Parameter Register. (See [Figure 26](#)).

## 6.7 Answer Start Of Frame

The PICC SOF must be compliant with the ISO14443 type-B, and is shown in [Figure 24](#)

- Ten or eleven Elementary Time Units (ETU) each containing a logical '0',
- Two ETUs containing a logical '1'.

**Figure 24. Answer Start Of Frame**

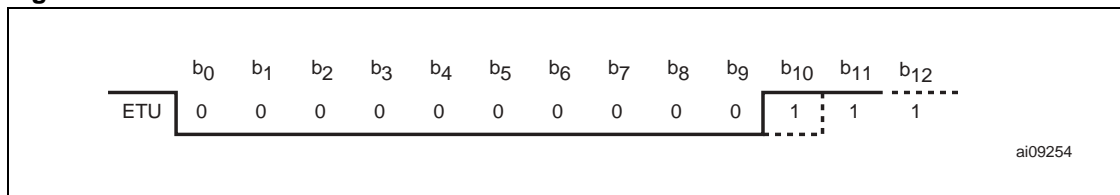


## 6.8 Answer End Of Frame

The PICC EOF must be compliant with the ISO14443 type-B, and is shown in [Figure 25](#):

- Ten or eleven Elementary Time Units (ETU) each containing a logical '0',
- Two ETUs containing a logical '1'

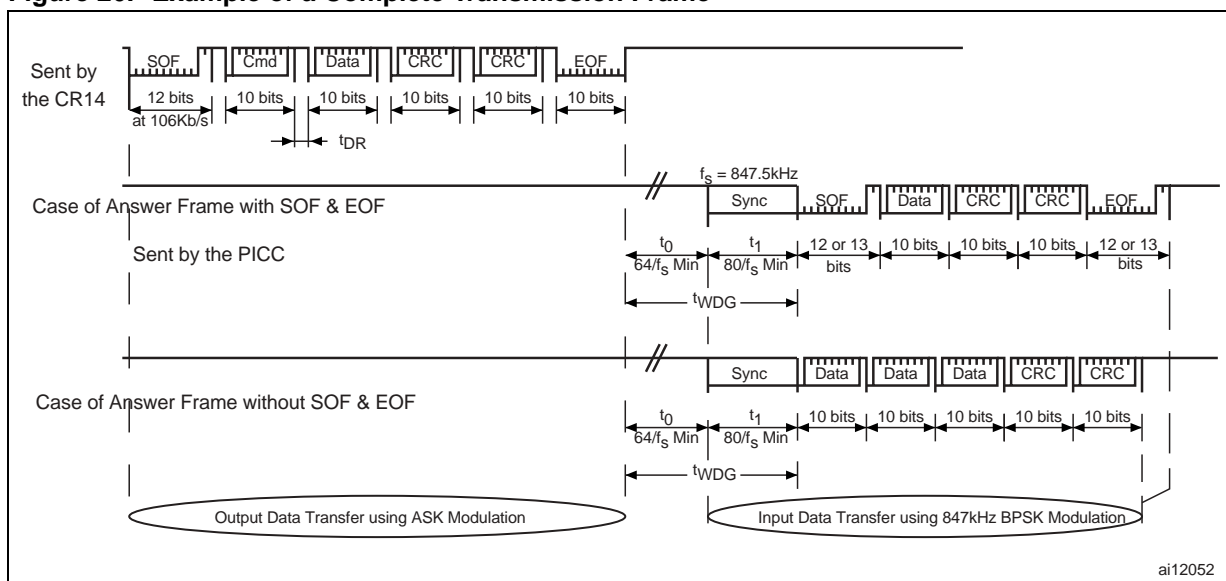
**Figure 25. Answer End Of Frame**



## 6.9 Transmission Frame

The Request Frame transmission must be followed by a minimum delay,  $t_0$  (see [Table 13](#)), in which no ASK or BPSK modulation occurs, before the Answer Frame can be transmitted.  $t_0$  is the minimum time required by the CR14 to switch from transmission mode to reception mode, and should be inserted after each frame. After  $t_0$ , the 13.56MHz carrier frequency is modulated by the PICC at 847kHz for a minimum time of  $t_1$  (see [Table 13](#)) to allow the CR14 to synchronize. After  $t_1$ , the first phase transition generated by the PICC represents the start bit ('0') of the Answer SOF (or the start bit '0' of the first data character in non SOF/EOF mode).

Figure 26. Example of a Complete Transmission Frame



## 6.10 CRC

The 16-bit CRC used by the CR14 follows the ISO14443 type B recommendation. For further information, please see [Appendix A on page 44](#).

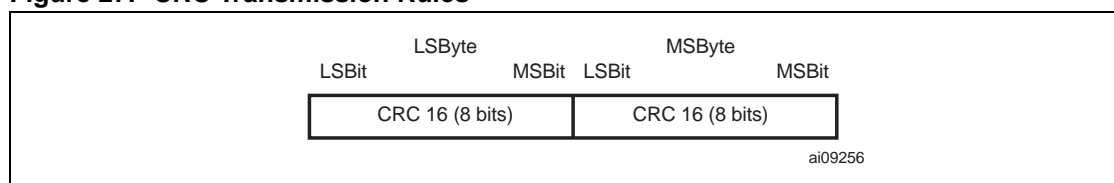
The two CRC Bytes are present in all Request and Answer Frames, just before the EOF. The CRC is calculated on all the Bytes between the SOF and the CRC Bytes.

Upon transmission of a Request from the CR14, the PICC verifies that the CRC value is valid. If it is invalid, it discards the frame and does not answer the CR14.

Upon reception of an Answer from the PICC, the CR14 verifies that the CRC value is valid. If it is invalid, it stores the value FFh in the Input/Output Frame Register.

The CRC is transmitted Least Significant Byte first. Each Byte is transmitted Least Significant Bit first.

Figure 27. CRC Transmission Rules



## 7 Tag access using the CR14 coupler

In all the following I<sup>2</sup>C commands, the last three bits of the Device Select Code can be replaced by any of the three-bit binary values (000, 001, 010, 011, 100, 101, 110, 111). These values are linked to the logic levels applied to the E2, E1 and E0 pads of the CR14.

### 7.1 Standard TAG Command Access Description

Standard PICC commands, like Read and Write, are generated by the CR14 using the Input/Output Frame Register.

When the host needs to send a standard frame command to the PICC, it first has to internally generate the complete frame, with the command code followed by the command parameters. Only the two CRC Bytes should not be generated, as the CR14 automatically adds them during the RF transmission.

When the frame is ready, the host has to write the request frame into the Input/Output Frame Register using the I<sup>2</sup>C write command specified in [Figure 13 on page 23](#). After the I<sup>2</sup>C STOP condition, the CR14 inserts the I<sup>2</sup>C Bytes in the required ISO character format ( [Figure 20](#)) and starts to transmit the request frame to the PICC. Once the RF transmission is over, the CR14 waits for the PICC to send an answer frame.

If the PICC answers, the characters received ([Figure 26](#)) are demodulated, decoded and stored into the Input/Output Frame Register, as specified in [Table 4](#). During the entire RF transmission, the CR14 disconnects itself from the I<sup>2</sup>C bus. On reception of the PICC EOF, the CR14 checks the CRC and reconnects itself to the I<sup>2</sup>C bus.

The host can then get the PICC answer frame by issuing an Input/Output Frame Register Read on the I<sup>2</sup>C bus, as specified in [Figures 14 and 15](#).

If no answer from the PICC is detected after a time-out delay, fixed in the Parameter Register (bits b<sub>5</sub> and b<sub>6</sub>), the Input/Output Frame Register is set as specified in [Table 4](#).

**Figure 28. Standard TAG Command: Request Frame Transmission**

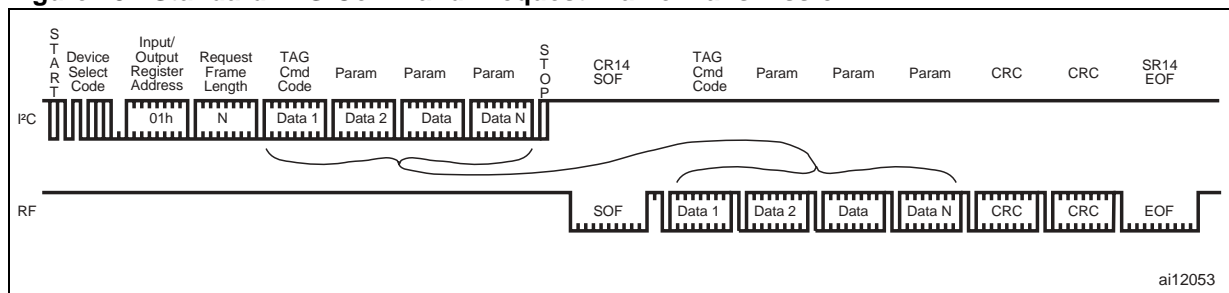


Figure 29. Standard TAG Command: Answer Frame Reception

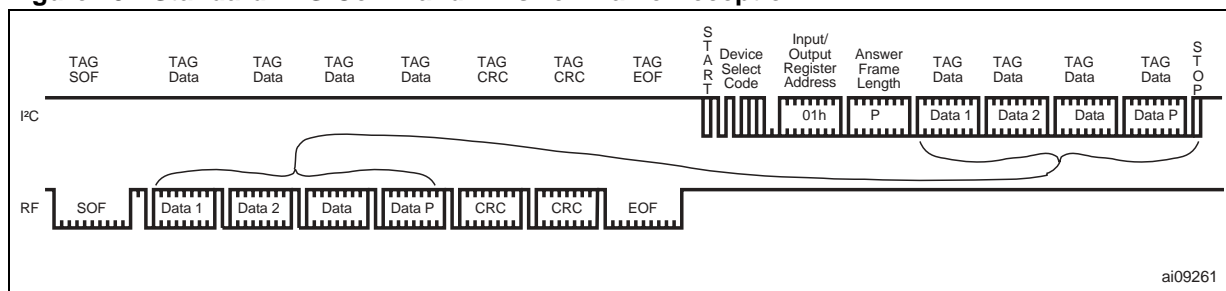
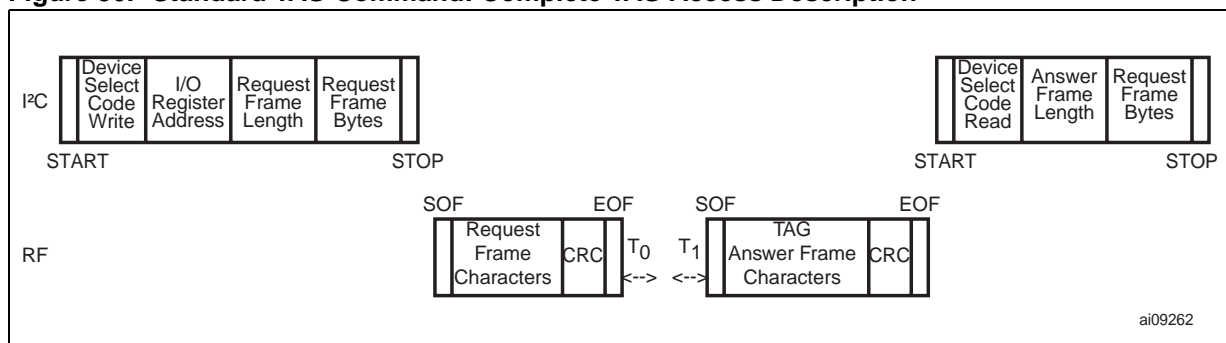


Figure 30. Standard TAG Command: Complete TAG Access Description



## 7.2 Anti-Collision TAG Sequence

The CR14 can identify an ST short range memory using a proprietary anti-collision system.

Issuing an I<sup>2</sup>C Write command to the Slot Marker Register ([Figure 16](#)) causes the CR14 to automatically generate a 16-slot anti-collision sequence, and to store the identified Chip\_ID in the Input/Output Frame Register, as specified in [Table 5](#).

After receiving the Slot Marker Register I<sup>2</sup>C Write command, the CR14 generates an RF PCALL16 command followed by fifteen SLOT\_MARKER commands, from SLOT\_MARKER(1) to SLOT\_MARKER(15). After each command, the CR14 waits for a tag answer. If the answer is correctly decoded, the corresponding Chip\_ID is stored in the Input/Output Frame Register. If there is no answer, or if the answer is wrong (with a CRC error, for example), the CR14 stores an error code in the Input/Output Frame Register. At the end of the sequence, the host has to read the Input/Output Frame Register to retrieve all the identified Chip\_IDs.



Figure 31. Anti-Collision ST short range memory Sequence (1)

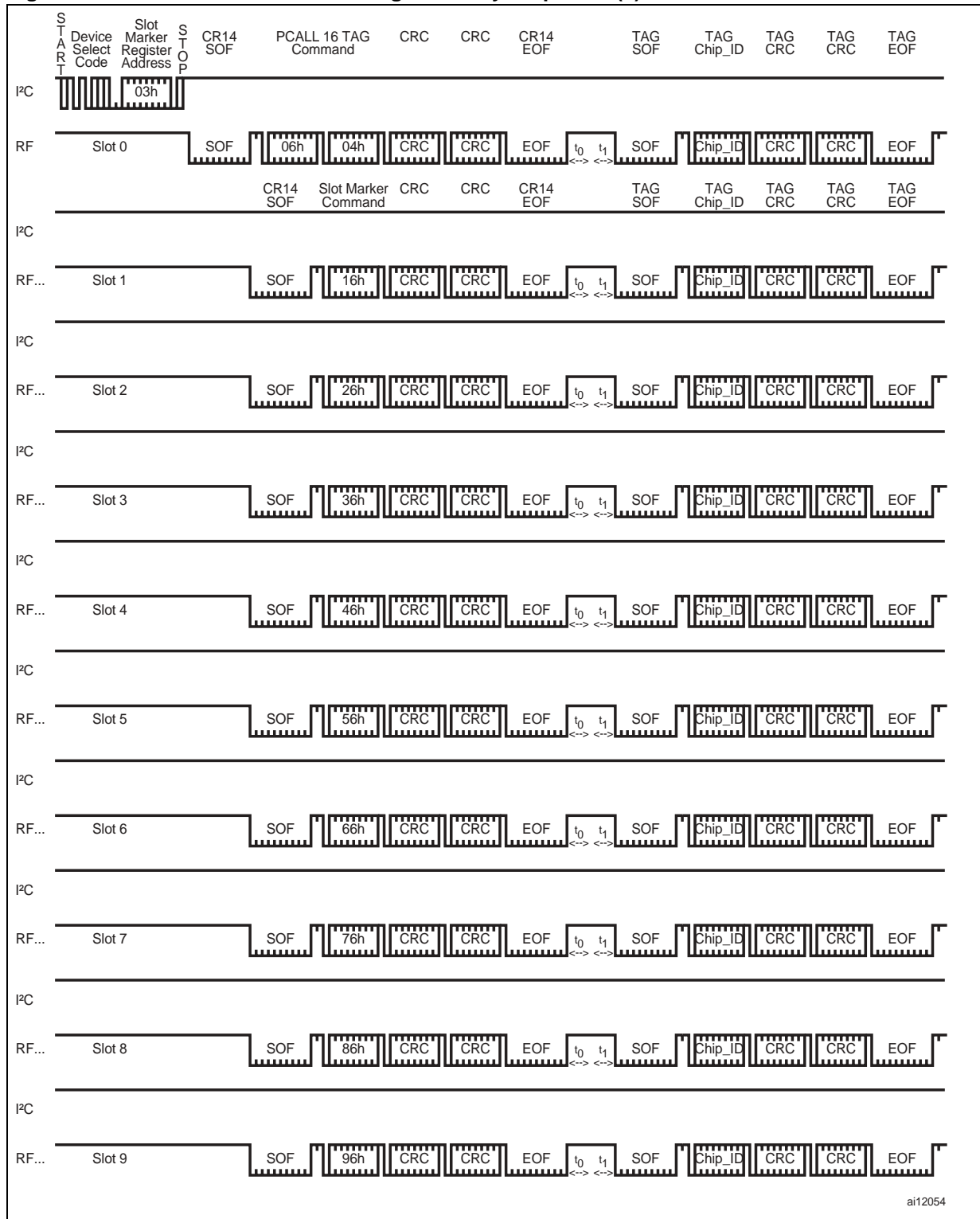
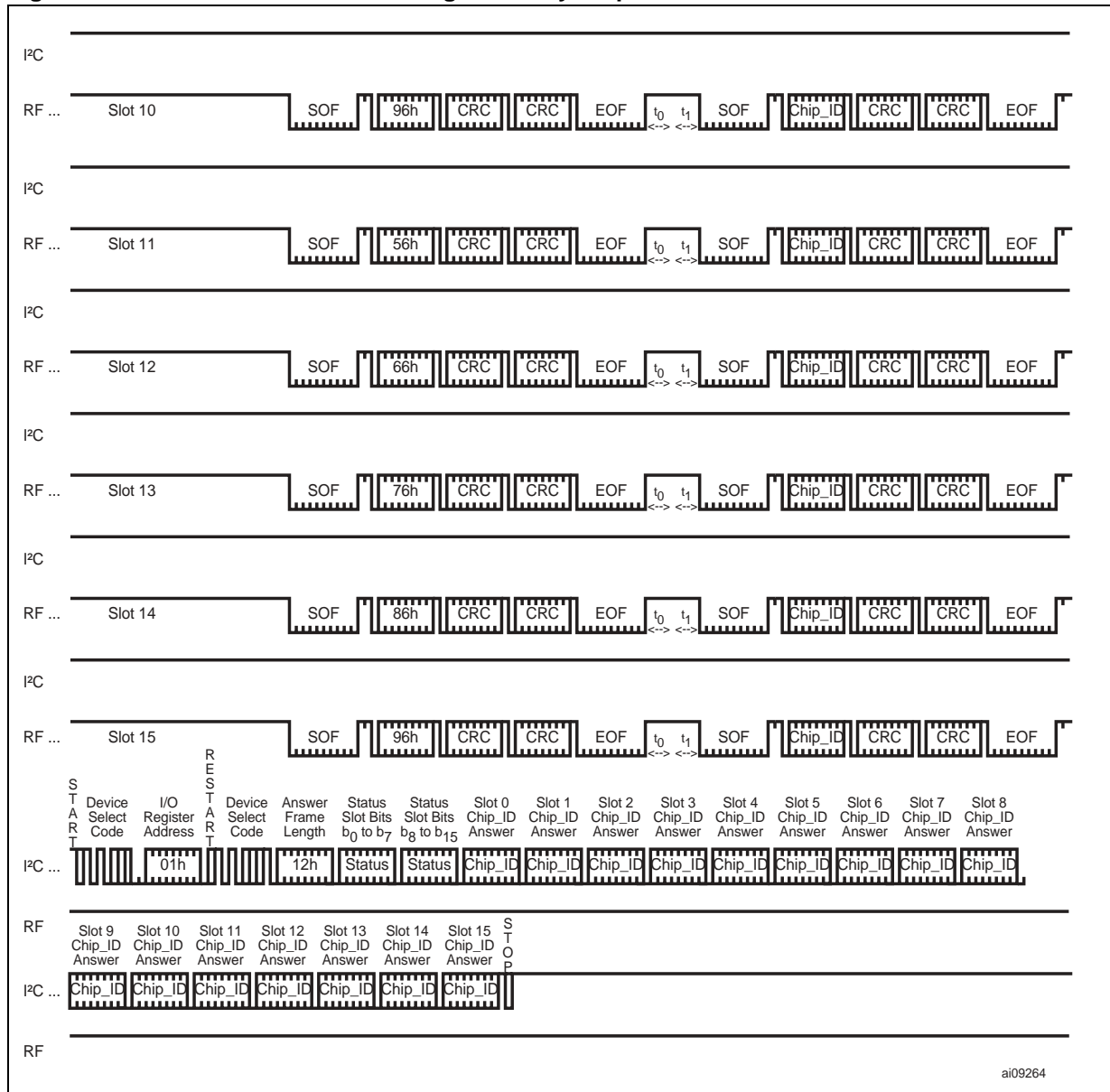


Figure 32. Anti-Collision ST short range memory Sequence Continued



## 8 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 8. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage Temperature	-65 to 150	°C
$V_{IO}$	Input or Output range (SDA)	-0.3 to 6.5	V
$V_{IO}$	Input or Output range (others pads)	-0.3 to $V_{CC}+0.3$	V
$V_{CC}$	Supply Voltage	-0.3 to 6.5	V
$P_{OUT}$	Output Power on Antenna Output Driver ( $RF_{OUT}$ )	100	mW
$V_{ESD}$	Electrostatic Discharge Voltage (Human Body model) <sup>(1)</sup>	4000	V
	Electrostatic Discharge Voltage (Machine model) <sup>(2)</sup>	500	V

1. MIL-STD-883C, 3015.7 (100pF, 1500Ω).

2. EIAJ IC-121 (Condition C) (200pF, 0Ω)

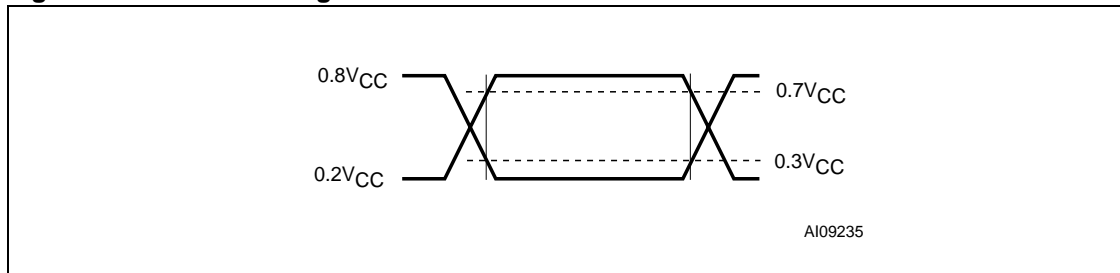
## 9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 9. I<sup>2</sup>C AC Measurement Conditions**

Parameter	Min.	Max.	Unit
V <sub>CC</sub> Supply Voltage	4.5	5.5	V
Ambient Operating Temperature (T <sub>A</sub> )	-20	85	°C
Input Rise and Fall Times		50	ns
Input Pulse Voltages	0.2V <sub>CC</sub>	0.8V <sub>CC</sub>	V
Input and Output Timing Reference Voltages	0.3V <sub>CC</sub>	0.7V <sub>CC</sub>	V

**Figure 33. I<sup>2</sup>C AC Testing I/O Waveform**



**Table 10. I<sup>2</sup>C Input Parameters<sup>(1,2)</sup>**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C <sub>IN</sub>	Input Capacitance (SDA)			8	pF
C <sub>IN</sub>	Input Capacitance (SCL, E0, E1, E2))			6	pF
t <sub>NS</sub>	Low Pass Filter Input Time Constant (SCL & SDA Inputs)		100	400	ns

1. Sampled only, not 100% tested.
2. T<sub>A</sub> = 25 °C, f = 400kHz.

Table 11. I<sup>2</sup>C DC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current (SCL, SDA, E0, E1, E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	μA
I <sub>LO</sub>	Output Leakage Current (SCL, SDA, E0, E1, E2)	$0V \leq V_{OUT} \leq V_{CC}$ . SDA in Hi-Z		±2	μA
I <sub>CC</sub>	Supply Current	$V_{CC} = 5V, f_C = 400kHz$ (rise/fall time < 30ns), RF OFF		6	mA
		$V_{CC} = 5V, f_C = 400kHz$ (rise/fall time < 30ns), RF ON		20	mA
I <sub>CC1</sub>	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 5V$ , RF OFF		5	mA
V <sub>IL</sub>	Input Low Voltage (SCL, SDA)		-0.3	0.3V <sub>CC</sub>	V
	Input Low Voltage (E0, E1, E2)		-0.3	0.3V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage (SCL, SDA)		0.7V <sub>CC</sub>	V <sub>CC</sub> + 1	V
	Input High Voltage (E0, E1, E2)		0.7V <sub>CC</sub>	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage (SDA)	I <sub>OL</sub> = 3mA, V <sub>CC</sub> = 5V		0.4	V

Figure 34. I<sup>2</sup>C AC Waveforms

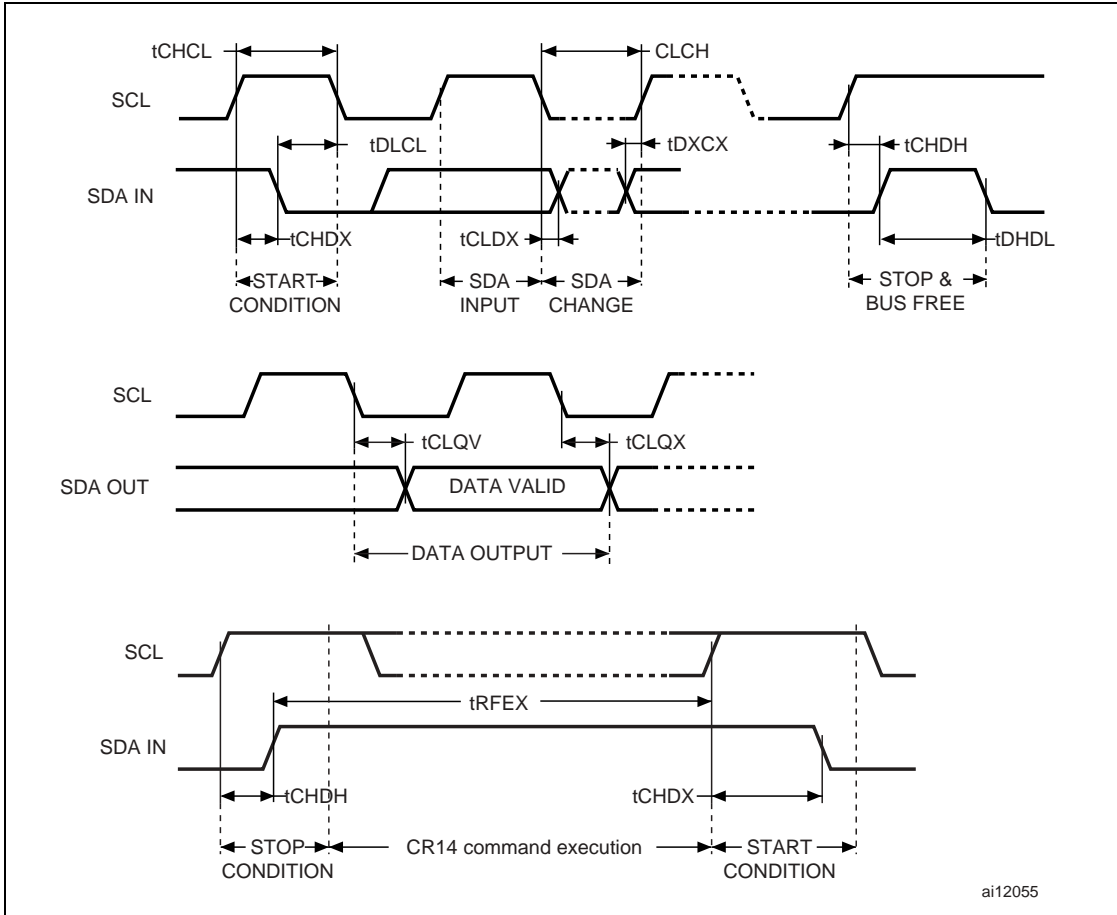
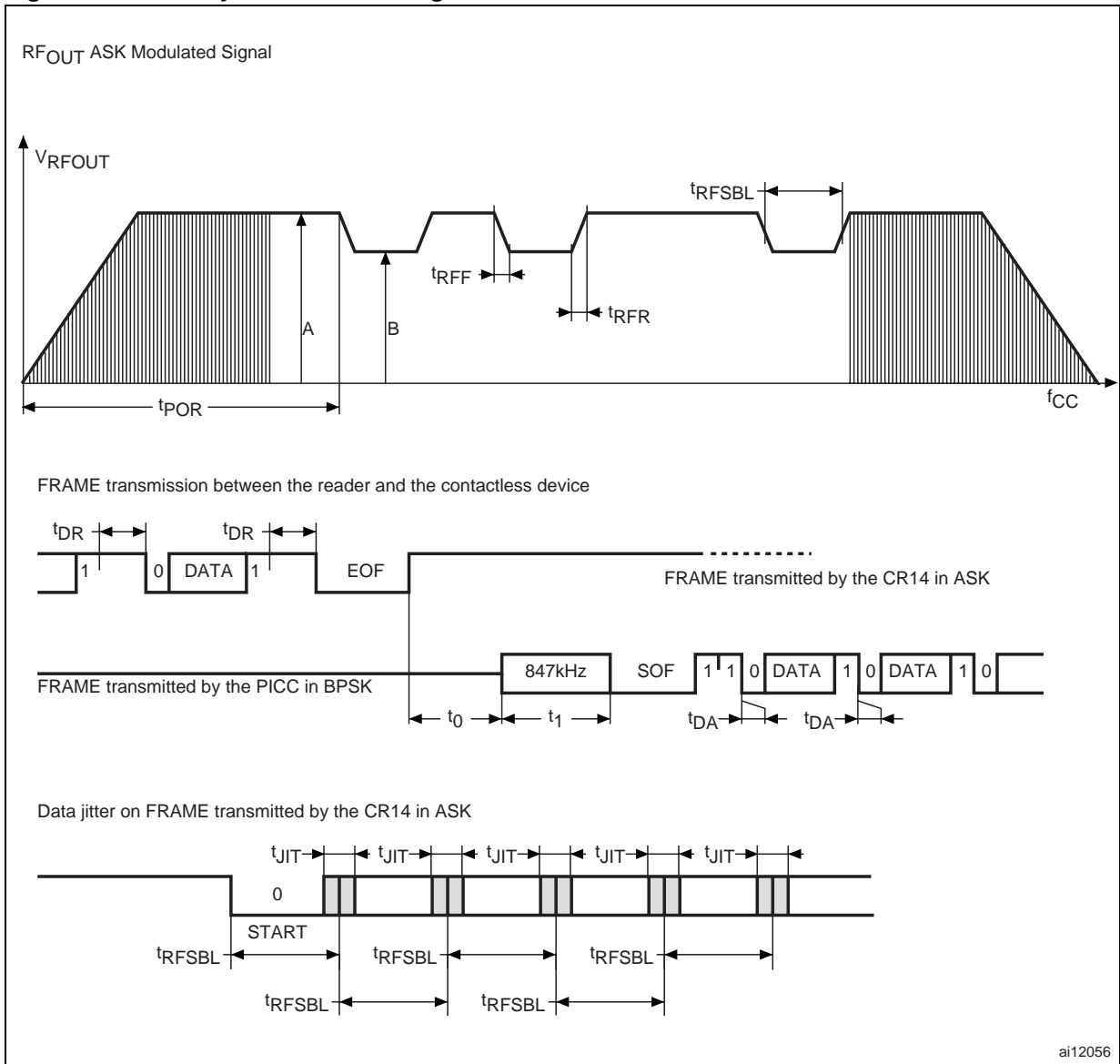


Table 12. I<sup>2</sup>C AC Characteristics

Symbol	Alt.	Parameter	Fast I <sup>2</sup> C 400 kHz		I <sup>2</sup> C 100 kHz		Unit
			Min	Max	Min	Max	
t <sub>CH1CH2</sub> <sup>(1)</sup>	t <sub>R</sub>	Clock Rise Time		300		1000	ns
t <sub>CL1CL2</sub> <sup>(1)</sup>	t <sub>F</sub>	Clock Fall Time		300		300	ns
t <sub>DH1DH2</sub> <sup>(1)</sup>	t <sub>R</sub>	SDA Rise Time	20	300	20	1000	ns
t <sub>DL1DL2</sub> <sup>(1)</sup>	t <sub>F</sub>	SDA Fall Time	20	300	20	300	ns
t <sub>CHDX</sub> <sup>(2)</sup>	t <sub>SU:STA</sub>	Clock High to Input Transition	600		4700		ns
t <sub>CHCL</sub>	t <sub>HIGH</sub>	Clock Pulse Width High	600		4000		ns
t <sub>DLCL</sub>	t <sub>HD:STA</sub>	Input Low to Clock Low (START)	600		4000		ns
t <sub>CLDX</sub>	t <sub>HD:DAT</sub>	Clock Low to Input Transition	0		0		μs
t <sub>CLCH</sub>	t <sub>LOW</sub>	Clock Pulse Width Low	1.3		4.7		μs
t <sub>DXCX</sub>	t <sub>SU:DAT</sub>	Input Transition to Clock Transition	100		250		ns
t <sub>CHDH</sub>	t <sub>SU:STO</sub>	Clock High to Input High (STOP)	600		4000		ns
t <sub>DHDL</sub>	t <sub>BUF</sub>	Input High to Input Low (Bus Free)	1.3		4.7		μs
t <sub>CLQV</sub>	t <sub>AA</sub>	Clock Low to Data Out Valid		1000		3500	ns
t <sub>CLQX</sub>	t <sub>DH</sub>	Data Out Hold Time After Clock Low	200		200		ns
f <sub>C</sub>	f <sub>SCL</sub>	Clock Frequency		400		100	kHz

1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

Figure 35. CR14 Synchronous Timing





**Table 13. RF<sub>OUT</sub> AC Characteristics**

Symbol	Parameter	Condition	Min.	Max.	Unit
f <sub>CC</sub>	External Oscillator Frequency	V <sub>CC</sub> = 5V	13.553	13.567	MHz
MI <sub>CARRIER</sub>	Carrier Modulation Index	MI=(A-B)/(A+B)	10	14	%
t <sub>RFR</sub> , t <sub>RFF</sub>	10% Rise and Fall time		0.5	1.5	μs
t <sub>RFSBL</sub>	Pulse Width on RF <sub>OUT</sub>	1 ETU = 128/f <sub>CC</sub>	9.44		μs
t <sub>JIT</sub>	ASK modulation bit jitter	CR14 to PICC	-0.5	0.5	μs
t <sub>0</sub>	Antenna Reversal delay	Min = 64/f <sub>S</sub>	75		μs
t <sub>1</sub>	Synchronization delay	Min = 80/f <sub>S</sub>	94		μs
t <sub>WDG</sub>	Answer delay watchdog (b <sub>5</sub> =0, b <sub>6</sub> =0)	Request EOF rising edge to first Answer start bit		500	μs
t <sub>WDG</sub>	Answer delay watchdog (b <sub>5</sub> =0, b <sub>6</sub> =1)			5	ms
t <sub>WDG</sub>	Answer delay watchdog (b <sub>5</sub> =1, b <sub>6</sub> =0)			10	ms
t <sub>WDG</sub>	Answer delay watchdog (b <sub>5</sub> =1, b <sub>6</sub> =1)			309	ms
t <sub>DR</sub>	Time Between Request characters	CR14 to PICC	9.44		μs
P <sub>A</sub>	RF <sub>OUT</sub> output power			90	mW
t <sub>POR</sub>	CR14 Power-On delay			20	ms

1. Data specified in the table above are estimated or target values. All values can be updated during product qualification.

**Table 14. RF<sub>IN</sub> AC Characteristics**

Symbol	Parameter	Condition	Min.	Max.	Unit
t <sub>RFSBL</sub>	PICC Pulse Width	1 ETU = 128/f <sub>CC</sub>	9.44		μs
f <sub>S</sub>	PICC Sub-carrier Frequency	f <sub>CC</sub> /16	847.5		KHz
t <sub>DA</sub>	Time Between Answer characters	PICC to CR14	1, 2, 3		ETU
V <sub>DYN</sub>	RF <sub>IN</sub> Dynamic Voltage Level	V <sub>DYN</sub> Max for V <sub>OFFSET</sub> = V <sub>CC</sub> /2	0.5	V <sub>CC</sub> /2	V
V <sub>OFFSET</sub>	RF <sub>IN</sub> Offset Voltage Level		2	3	V
V <sub>RET</sub>	RF <sub>IN</sub> Retro-modulation Level		120		mV

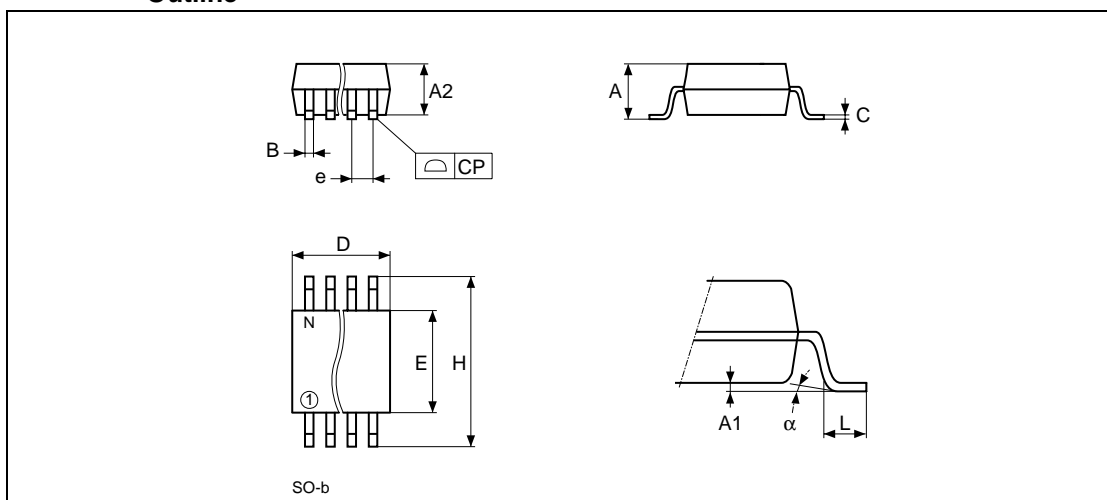
1. Data specified in the table above are estimated or target values. All values can be updated during product qualification.

# 10 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 36. SO16 Narrow - 16 lead Plastic Small Outline, 150 mils body width, Package Outline**



1. Drawing is not to scale.

**Table 15. SO16 Narrow - 16 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data**

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
a		0°	8°		0°	8°
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
CP			0.10			0.004
D		9.80	10.00		0.386	0.394
e	1.27	–	–	0.050	–	–
E		3.80	4.00		0.150	0.157
L		0.40	1.27		0.016	0.050
N	16			16		

# 11 Part numbering

**Table 16. Ordering Information Scheme**

Example:	CR14	-	MQ	/	XXX
<b>Device Type</b>	CR14				
<b>Package</b>			MQ = SO16 Narrow (150 mils width) MQP = SO16 Narrow (150 mils width) ECOPACK®		
<b>Customer Code</b>					XXX = Given by the issuer

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

## Appendix A ISO14443 type B CRC calculation

```

#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTEunsigned char
#define USHORTunsigned short
unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
    ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
    ch = (ch^(ch<<4));
    *lpwCrc = (*lpwCrc >> 8)^((USHORT)ch <<
8)^((USHORT)ch<<3)^((USHORT)ch>>4);
    return(*lpwCrc);
}
void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE
*TransmitSecond)
{
    BYTE chBlock; USHORTt wCrc;
    wCrc = 0xFFFF; // ISO 3309
    do
    {
        chBlock = *Data++;
        UpdateCrc(chBlock, &wCrc);
    } while (--Length);
    wCrc = ~wCrc; // ISO 3309
    *TransmitFirst = (BYTE) (wCrc & 0xFF);
    *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
    return;
}
int main(void)
{
    BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
    printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1");
    printf("CRC_B of [ ");
    for(i=0; i<4; i++)
        printf("%02X ",BuffCRC_B[i]);
    ComputeCrc(BuffCRC_B, 4, &First, &Second);
    printf("] Transmitted: %02X then %02X.", First, Second);
    return(0);
}

```

## 12 Revision history

**Table 17. Document Revision History**

Date	Version	Revision Details
16-Dec-2005	1	Initial release.

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